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Residual Stress in CVD-grown 3C-SiC Films on Si Substrates

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ABSTRACT

Having superior mechanical properties, 3C-SiC is one of the target materials for power MEMS applications. Growing 3C-SiC films on Si is challenging, as there is a large mismatch in lattice parameter and thermal expansion between the SiC film and the Si substrate that needs to be accommodated, and results in high residual stress. Residual stress control is critical in MEMS devices as upon feature release it results in substantial deformation.

3C-SiC single crystalline films were deposited on 50 mm (100) and (111) Si substrates in a hot-wall CVD reactor. The film tensile residual stress was so high that it fractured on the (111) Si wafer. The resulting film thickness on the (100) Si wafer was non-uniform, having a linear profile along the growth direction. This presented a challenge of using the substrate curvature method for calculating residual stress. Finite Element Method correction was applied to the Stoney's formula for calculating the residual stress along the wafer radius. Suggestions for reducing the amount of residual stress are made.

INTRODUCTION

SiC is the material of choice for power MEMS applications, since it has much better mechanical performance at high temperatures, compared to Si. Deposition and processing techniques must be mastered before a functioning device can actually be built. It is advantageous to deposit SiC on Si wafers due to their high quality and low cost, in comparison to SiC substrates. However, one has to overcome the 22% lattice mismatch between the 3C-SiC film and the (100) Si substrate, and additional 8% mismatch in thermal expansion. Any temperature variation will cause stress. 3C-SiC films on (111) Si wafers have larger residual stress, although there is a slightly smaller lattice mismatch of about 19.7%. In both instances 3C-SiC can be hetero-epitaxially grown on a highly defective SiC buffer layer formed during the so-called carbonization step, which could accommodate some of the mismatch strain.

EXPERIMENT

Single crystal 3C-SiC films were grown hetero-epitaxially in a hot-wall chemical vapor deposition (CVD) reactor on (100) and (111) 50 mm Si substrates [1]. The 3C-SiC on Si deposition process was developed using the two step carbonization and growth method. C_3H_8 and SiH_4 were used as the precursors to provide the carbon and silicon sources, respectively. The carrier gas was ultra-high purity hydrogen, purified in a palladium diffusion cell. Prior to growth, the substrates were prepared using the RCA cleaning method [2], followed by a 30 second immersion in diluted hydrofluoric acid to remove the surface oxide and possible contaminants.

The samples were then thoroughly dried in N_2 and loaded into the CVD reactor, which was then evacuated of all residual gases prior to processing.

The carbonization process step involved heating either the (100) Si or the (111) Si substrate from room temperature to 1135 °C at 400 Torr pressure in a flow of 16 standard cubic centimeters per minute (sccm) of C_3H_8 and 10 standard liters per minute (slm) of H_2. This temperature was maintained for two minutes to carbonize the substrate surface. After carbonization, the temperature was gradually ramped to 1380 °C, which began the growth stage. During the ramp, the propane flow was linearly decreased to 8.0 sccm for a (100) Si substrate or to 5.6 sccm for a (111) Si substrate. A 10% silane/hydrogen mixture (SiH_4), which is the silicon precursor, was slowly added until a final flow rate of 270 sccm was achieved at the end of the second thermal ramp when using a (100) Si substrate. When growing on (111) Si, the 10% silane/hydrogen mixture flow rate was linearly increased during the second ramp to a final value of 218 sccm. The silicon to carbon ratio, Si/C, for the growth stage was 1.13 and 1.30 for (100) Si and (111) Si, respectively. For growth on a (100) Si wafer, the pressure was reduced from 400 to 100 Torr and the hydrogen flow was linearly increased to 30 slm at 65 °C before the ramp was completed in order to transport the cracked growth species more effectively to the growth zone located 60 mm upstream from the hot-zone outlet. However, for (111) Si, the pressure was maintained at 400 Torr and the hydrogen flow was increased to 40 slm at 1320 °C. The temperature and gases flow were then held constant at the end of the second ramp, allowing the continuous epitaxial growth of 3C-SiC on the carbonized Si buffer layer [3]. After the growth process was completed, the wafer was cooled to room temperature in an Ar atmosphere [4]. The process flow is shown schematically in Figure 1, and the details of both the reactor construction and the growth process can be found in reference [5].

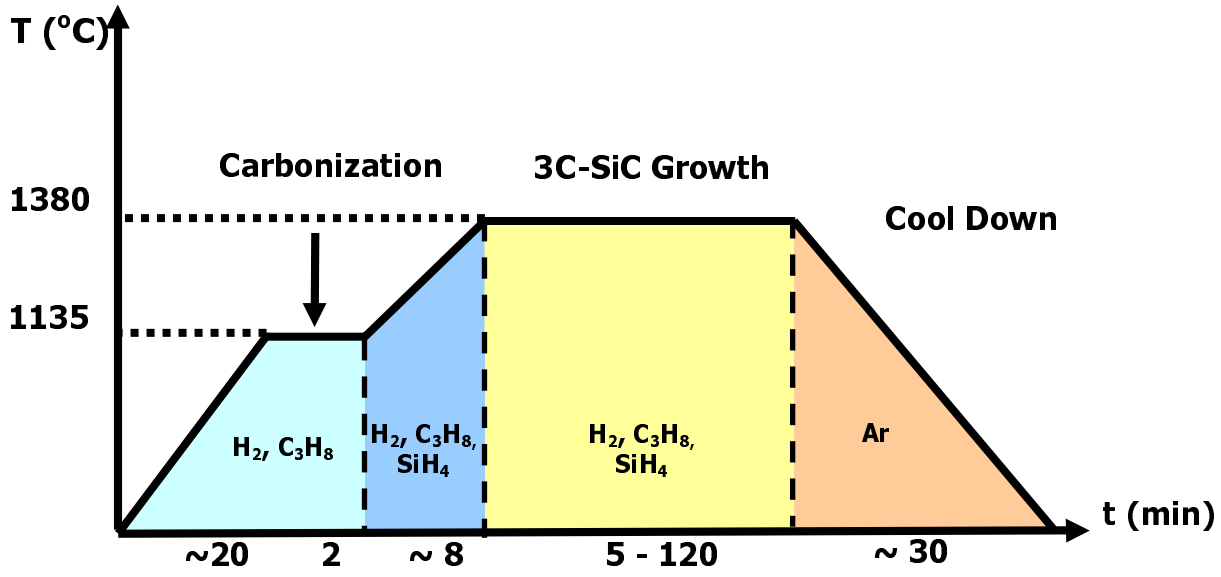

Figure 1. Single crystal 3C-SiC films growth process [5]. The resulting growth rate was 10 μm/h.

The crystal orientation of the grown films was determined by X-ray diffraction (XRD) using a Philips X-Pert X-ray diffractometer. Figure 2 shows powder (θ-2θ) scans obtained from

SiC films grown on (100) and (111) Si substrates. The orientation of the single crystal SiC film is (100) on (100) Si wafers and (111) on (111) Si wafers. The (100) 3C-SiC film is of higher quality, as it exhibits a sharp (200) peak, while the (111) 3C-SiC film peak on the (111) Si wafer was split into three peaks due to the high residual stress and its relief. This stress caused visible (111) Si wafer curvature and was partially relieved by film fracture and delamination, causing a triple peak. XRD rocking curve data on the (100) 3C-SiC film showed that the films were single crystal with an X-ray rocking curve peak full width half maximum (FWHM) of approximately 300 arcseconds [5, 6].

Mechanical properties of 3C-SiC on (100) Si were measured, and it was determined that single crystalline films have an elastic modulus of 430 GPa and a hardness of 30 GPa [6]. The elastic properties data was used for the Finite Element Modeling. The mechanical properties of the polycrystalline films were slightly higher, making them more attractive for power MEMS applications.

In the reactor used for the growth no wafer rotation is available, therefore the film thickness varied substantially across the wafer. Figure 3a shows interference fringes originating from the film thickness non-uniformity and the (100) Si wafer curvature due to residual stress observed when using 1/10 wave optical flat on the 50 mm wafer. Vertical film thickness profile is presented in Figure 3b obtained from an Accent QS-1200 Fourier transform infrared spectrometer (FTIR). The thickness measurements were taken along the wafer diameter starting from the primary flat and ending on the opposite wafer side. Using the FTIR graduated mounting stage, each thickness measurement was made in 5 mm intervals.

The gases were introduced from the top of the wafer, which was specified in these experiments as the side of the wafer opposite the primary wafer flat, resulting in a linear film thickness profile along the y direction (Figure 3b).

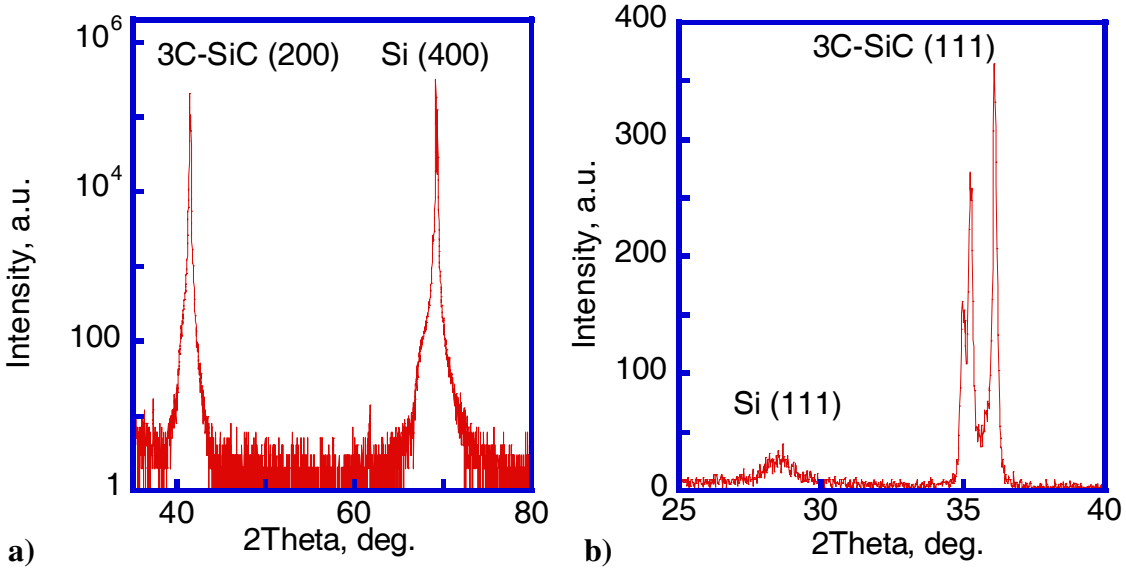

Figure 2. XRD powder (θ-2θ) scan for 3C-SiC films grown on a) (100) and b) (111) Si substrates. In both instances the films are single crystalline, with the (111) film having triple peak due to high residual stress and its relief by fracture.

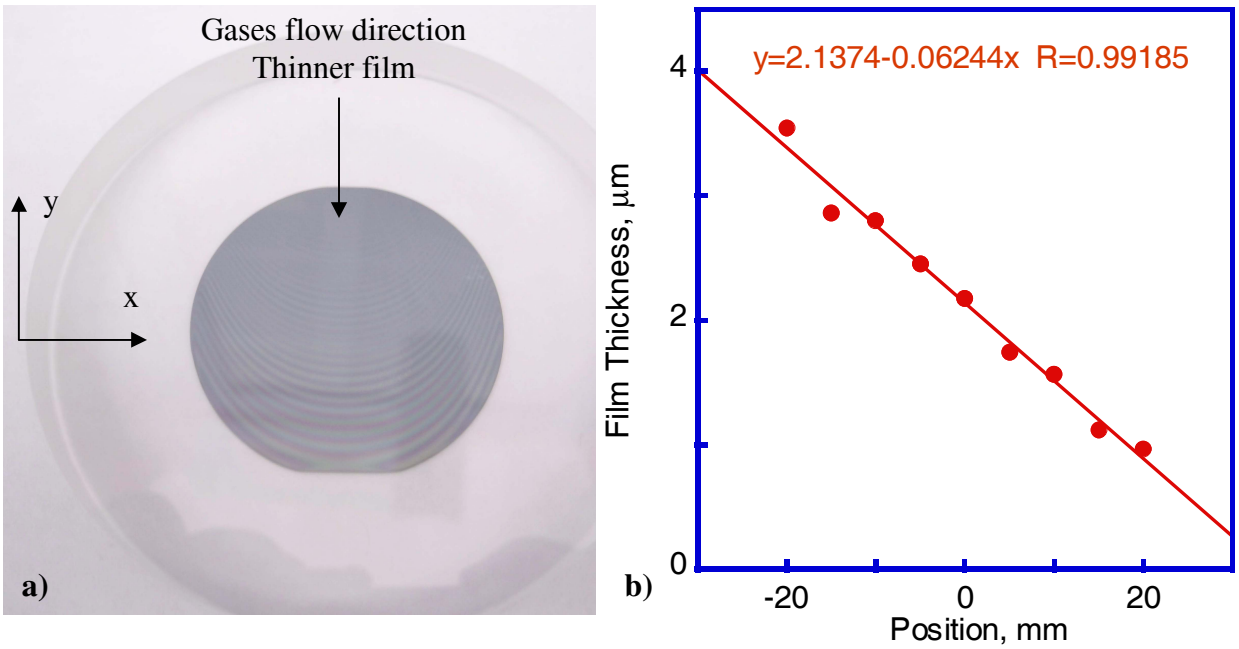

Figure 3. a) Photograph of the 50 mm (100) Si wafer with 3C-SiC film showing interference fringes due to film thickness non-uniformity and wafer curvature; b) 3C-SiC film thickness vertical profile measured using FTIR spectrometry.

DISCUSSION

The assumption of the original Stoney formulation implies that there is a uniform film thickness across the wafer and that the curvature is axisymmetric. These assumptions are obviously violated in our case of non-uniform film thickness distribution. In view of this fact, residual stress in the 3C-SiC film grown on the (100) 525 µm thick Si substrate was calculated based on the wafer curvature change after film deposition utilizing the Stoney equation [7] with a correction factor:

$$\sigma_R(r) = \frac{E_s}{1-\nu_s}\frac{\Delta k(r) h_s^2}{6h_f(r)} c(r) \qquad (1),$$

where $\Delta k(r)$ is the radius-dependent difference in wafer curvature before and after film deposition, E_s and ν_s are the substrate elastic modulus and Poisson's ratio, respectively, h_s is the substrate thickness, $h_f(r)$ is the film thickness and $c(r)$ is the correction factor as a function of the wafer radial position. The correction factor was calculated from an axisymmetric FE model of the wafer with experimentally measured film thickness distribution (see Fig. 3b). After applying a dummy uniform film stress to the model, the relative difference between the curvature calculated by the Stoney's formula and the FEM can be obtained, giving the correction factor. It turns out that the Stoney's formula overestimates the stress by over 7-10% for the 50% film thickness variation across the wafer (Figure 4a). Figure 4b shows the residual stress profile of

3C-SiC film in the vertical direction calculated based on the wafer curvature change and the FEM correction to the Stoney's formula. The stress ranges from 215 to 450 MPa across the 50 mm wafer diameter.

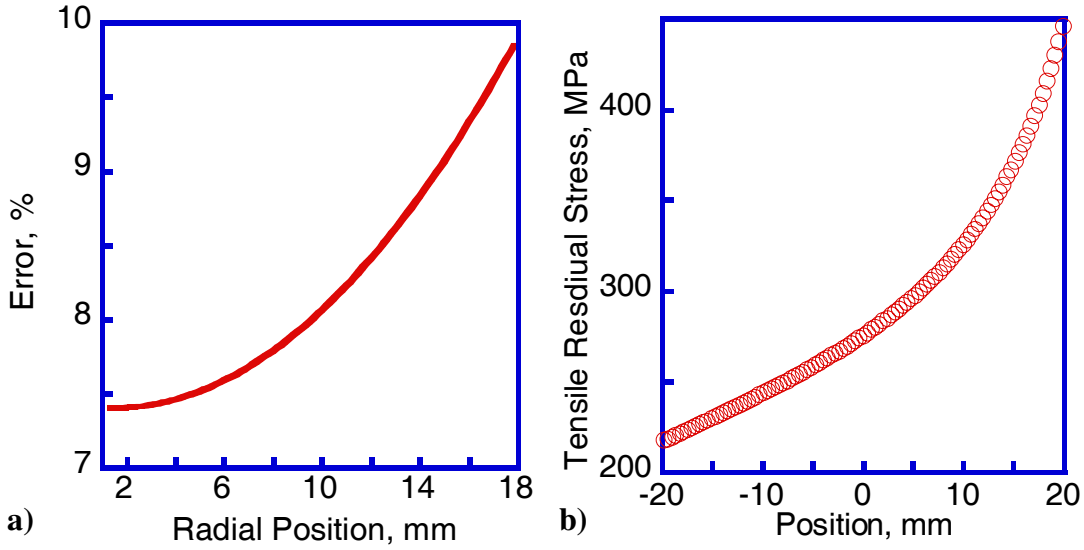

Figure 4. a) FEM correction to the Stoney's formula for the measured film thickness variation; b) Residual stress in the 3C-SiC film grown on (100) Si substrate based on the curvature method with the FEM correction.

The 2D finite element correction assumed that the curvature change is axisymmetric, which is also not the case. Further model development is needed to provide a 3D solution. In the middle of the wafer the tensile equibiaxial stress is 265 MPa. The (111) Si wafer curvature after 3C-SiC film growth was not measured because the film fractured due to the high tensile residual stress relief. Wafer curvature was noticeable to the naked eye. The wafer warped upwards indicating tensile residual stress in the film.

Numerous approaches have been investigated to reduce the lattice mismatch between 3C-SiC and Si. One of the problems is that SiC does not alloy, as is the case of the SiGe system for example. While buffer layers are used in all known SiC growth processes, the so-called carbonization step produces a highly defective buffer layer, which helps accommodate the misfit. Unfortunately it can not help in reducing the thermal stresses. Complaint substrates have been investigated using porous Si buffer layers [8], nano-grooved surfaces [9], and recent work has focused on growing 3C-SiC on oxide layers to provide strain relief [10]. One method used in our reactor to achieve a more uniform film thickness is to mechanically rotate the wafer by 180° and continue the growth. This has resulted in a highly uniform film thickness but the stress is unknown at this point. These films are being studied as per this paper and the results will be provided in the near future.

CONCLUSIONS

3C-SiC thin films deposited on Si wafers for MEMS applications have large residual tensile stress that varies substantially across the 50 mm wafer diameter, from 215 to 450 MPa. CVD process needs to be optimized to reduce the residual stress, which will cause large MEMS device deformations upon release. The stress was estimated based on the 2D FEM correction to the Stoney equation for the 50% film thickness variation.

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