EEL 5344C: CMOS VLSI Design
Fall 2008 Assignment No. 1
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Due Date: 1st October, 2008, in class.

Objective
You will familiarize yourself with the *virtuoso* layout system available in CADENCE VLSI design tool suite.

Details
Draw the layout of the following complementary CMOS gates/components using *virtuoso*. Follow DRC rules and verify the circuit functionality by simulation using HSPICE. **You should minimize your design dimensions following DRC rules.** You need to write test vectors to simulate and verify the functionality of the circuit. Verify exhaustively, where ever possible.

You should *not* use any cells from the standard CMOS library available (if any) within the CADENCE system. You may want to look at the layouts suggested in the Weste & Eshragian book.

1. (5 pts.) Basic inverter cell.
2. (5 pts.) 2-input NAND gate
3. (5 pts.) One-bit full adder cell.
4. (5 pts.) Using the basic adder cell, design an 4-bit ripple carry adder.

In the report, provide
(1) Schematic diagram,
(2) Printout of the simulation results (Exhaustive where ever possible),
(3) Printout of the layout diagram.
(4) HSPICE model for simulation as well as the input test vectors,
(5) The number of lab hours spent, and level of difficulty (easy, reasonable, difficult, very difficult)).

Important Notice
Do not discard your designs upon completion of the assignment!! They will be used as the starting point in the subsequent assignments!!

Good Luck!!