EEL 4705; Logic Design
Spring 2008; Monday 6:00pm-9:00pm; CHE 217

Instructor: Dr. Sanjukta Bhanja
Office: ENB 376/349A
Phone: 974-4755/974-4477
Office Hours: TR 11.00 am - 12:00 noon
Email: bhanja@eng.usf.edu

Teaching Assistant: Not available

Objectives: To make the student a skilled Logic designer – is the sole objective of this course.

Course Textbook:

Bibliography:


Grade Distribution:
Test1: 25%  Test2: 35%  In Class Surprise Quizzes: 40%

Topics:
- Introduction and overview of digital computers
- Number system, Computer Arithmetic
- Boolean Algebra
- Combinational circuits
- Boolean Logic manipulation
- Logic Design and Programmable Logic
- Flip-Flops
- Synchronous sequential circuits
- State Machines
- Asynchronous sequential circuits
- CMOS families

Special Notes:
- Academic dishonesty will not be tolerated and the student, in question, will be dealt with in accordance with the departmental policies.
- If you need any special accommodation according to the American Disability Act, please let me know.
- Make-up exams are only permitted only if it is a reasonable excuse, you inform me in a timely fashion, and you document your excuse. No make-up for the Surprise quizzes will be allowed but the grading will be based on the best 2/3 of the total quizzes.
- Students who anticipate the necessity of being absent from class due to the observation of a major religious observance must provide notice of the date(s) in writing by the second class meeting.