LOW POWER VLSI DESIGN (EEL 6936-002)

Instructor: Dr. SanjuktaBhanja Spring 2007

Lecture: ENG 003, MW 3:30-4:45 pm Office: ENB 376, ENB 349A; Office Hours: MW 1:15-2:15 pm Email: bhanja@eng.usf.edu Phone: 9744755/9744477 Prerequisites: CMOS VLSI Design

Text Books:

- "LOW-POWER CMOS VLSI CIRCUIT DESIGN" by Kaushik Roy and Sharat C. Prasad, published by Wiley-Interscience, ISBN # 047111488-X
- ``CMOS Low Power Digital Design," A. Chandrakasan & R. Brodersen, Kluwer Academic Pubs. 1995.
- ``Low Power Design Methodologies," J. Rabaey & M. Pedram (Editors), Kluwer Academic Pubs. 1996.

Objectives:

In recent years, enormous growth has occurred in terms portability of the computation. Computing demands from battery operated devices are increasing rapidly. This course is targeted to capture all the information regarding the existing techniques and future challenges for CMOS VLSI design that consumes low power. Towards the end, we want to focus on issues that are dominant in low power design under nano domain. The first objective is to study power estimates at various levels of abstraction, namely RT level, Logic level, behavioral and Software level. Next, we would cover low power synthesis and optimization techniques. We would conclude with low voltage design styles with increasing emphasis on leakage power, interconnects, reliability.

Grade Distribution:

Test1: 20%; Test2: 25%; Term paper: 15%; Assignments: 10%; Test3: 30%

Assignments:

You would require to use CADENCE tool suite and HSPICE.

Grading Policies:

A: 90% and above, B: 80 % and above, C: 70% and above. Students found guilty of academic misconduct will get "F" grade according to the departmental policy.

Main Topics:

- Power dissipation in Long-channel and submicron MOSFET and Challenges in low power VLSI design
- Power estimation: Probabilistic techniques, statistical techniques and simulative methods.
- Power estimation for combinational and sequential circuits
- Power estimation at various levels.
- Maximum power estimation
- Power optimization: behavioral level, logic level and circuit level optimization
- Low supply voltage based design
- Low power memories
- Energy recovery techniques.