EEL 6936-002: Low Power CMOS VLSI DESIGN
Spring 2003; Test No. 1–Make-up
Instructor: Sanjukta Bhanja
Friday March 7, 2003
3:00pm – 4:30pm

NOTE:

This is a closed text and closed notes exam. There will be partial credits. Total points you can get is 25. Any effort of academic dishonesty will be severely penalized.

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1. Do not exceed more than three simple sentences in answering each questions in this group.

   Describe the relationship between power dissipation and temperature. (2 pts)
   Describe the effect of load capacitance on short circuit power. (1 pt)
   What is the key (most important) difficulty in estimation for sequential circuit? (2 pts)
   What are the factors that should be taken into account for peak power estimation? (2 pts)
   What is a dynamic hazard? (2 pts)
   Define transition density? (1 pt)

2. Draw a BDD for the following boolean expression without reducing it (3 pts)

$$f = x_1 x_2^{'} x_3^{'} + x_3 x_2 + x_1^{'} x_2 \tag{1}$$

   What should be the chosen order of variables in BDD construction to obtain maximum efficiency? (1 pt)
   Calculate signal probability of f through the BDD. (1 pt)

3. Assume that all gate have the same delay d in Eq.1, Compute $P(f(T+2d))$ and compute switching probability at time $(T+3d)$ where signal x_1, x_2, x_3 are synchronous and arrive at time T. (2+4 pts)

4. Draw the ESTG based on the following STG? (4 pts)
   $s_0 \rightarrow s_1$ *on input* $'0'$, $s_1 \rightarrow s_2$ *on input* $'1'$
   $s_0 \rightarrow s_3$ *on input* $'1'$, $s_1 \rightarrow s_4$ *on input* $'0'$
   $s_4 \rightarrow s_4$ *on input* $'0'$, $s_4 \rightarrow s_3$ *on input* $'1'$
   $s_3 \rightarrow s_1$ *on input* $'0'$, $s_3 \rightarrow s_0$ *on input* $'1'$
   $s_2 \rightarrow s_0$ *on input* $'1'$, $s_2 \rightarrow s_3$ *on input* $'0'$

◇◇ Good Luck !! ◇◇