EEL 6936-002: Low Power VLSI DESIGN
Spring 2004; Midterm 2
Instructor: Sanjukta Bhanja
April 12, 2004
Due by April 21, 2004

NOTE:

Total points you can get is 25. **All the values not provided here, should be assumed with an Engineering judgment and clearly stated**. Any effort of academic dishonesty will be severely penalized.

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1. For a two input NAND gate compute sub-threshold leakage current I_{sub} for each of the four input combination. Assume that the threshold voltage is .1% of the last three digits of you SSN. If this number is greater than 0.7, subtract 0.5 from it for a reasonable threshold voltage or if it is less than 0.2 assume 0.2 Volts as threshold voltage. Assume V_{dd} as 2.0 volt. (10 pts)

2. Calculate Average Rise time and Fall time for the two input NAND gate and average gate delay. (7 pts)

3. If you reduce V_{dd} from 2.0 volts to 1.6 volts, what would be the change in threshold voltage for maintaining the same delay as calculated in the last question? What would be the change in leakage power in this case? (8 pts)

◇◇ Good Luck !! ◇◇