Bayesian Macromodeling for Circuit Level QCA Design

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***Abstract*—We present a probabilistic methodology to model and abstract the behavior of quantum-dot cellular automata circuit(QCA) at "circuit level" above the current practice of layout level. These macromodels provide input-output relationship of components (a set of QCA cells emulating a logical function) that are faithful to the underlying quantum effects. We show the macromodeling of a few key circuit components in QCA circuit, such as majority logic, lines, wire-taps, cross-overs, inverters, and corners. In this work, we demostrate how we can make use of these macromodels to abstract the logical function of QCA circuits and to extract crucial device level characteristics such as polarization and low-energy error state configurations by circuit level Bayesian model, accurately accounting for temperature and other device level parameters. We also demonstrate how this macromodel based design can be used effectively in analysing and isolating the weak spots in the design at circuit level itself.**

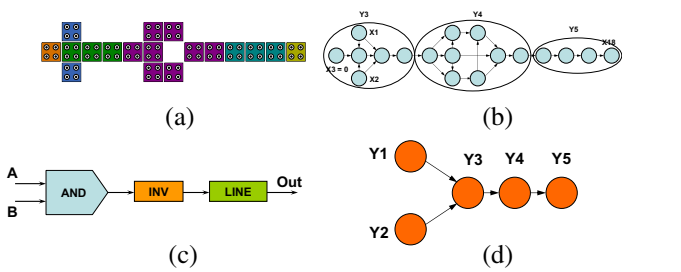


Fig. 1. A NAND gate (a) QCA layout (b) Bayesian model of QCA layout (c) Macromodel block diagram (d) Bayesian model of macromodel block diagram.

I. Introduction

Quantum-dot Cellular Automata (QCA) technology offers a new computing paradigm at nano-level [1], [2]. Several novel QCA designs have been proposed using unconventional architectural schemes [3]. While a lot of work has been done to explore layout level issues [4], [5], [6] in QCA, it is necessary to look beyond the layout level and explore circuit level issues so as to scope out the types of circuits that can be built. One of the most important paradigms for complex CMOS circuit design is a hierarchical design scheme that extracts essential design parameters at various levels of abstraction, such as architectural, circuit, layout, and device levels. This work intends to build a similar design structure for QCA by proposing a hierarchical design methodology for QCA circuits based on majority gates and other logic components, emphasizing the probabilistic and quantum mechanical nature of the operations at nano-level. Henderson *et al.* [7] proposed an hierarchical CMOS-like top-down approach for QCA blocks that are analyzed in terms of 0-1 boolean logic and hence is not able to capture the inevitable uncertainity issues that are quite apparent when working at nano-level.

In this work, we demonstrate a hierarchical design methodology that enables one to characterize designs with respect to thermal profiles and errors, by making use of probabilistic macromodels. A Bayesian modeling scheme is proposed to illustrate standard QCA circuit elements such as majority logic, lines, wire-taps, cross-overs, inverters, and corners using conditional probability distributions defined over the output states *given* the input states. The full circuit level model is constructed by chaining together the individual logic element macromodels. This circuit represented using the graphical probabilistic models known as Bayesian networks, where the nodes of the graphs are the individual macromodels and the links represent the connection between them. Each node is quantified by the macromodel conditional probabilities. The complete network represents a joint probability distribution over the whole circuit. Since conditional distribution over the inputs and outputs are obtained based on quantum mechanical probabilistic characterization, the circuit level model is also faithful to the underlying quantum-mechanical phenomena. This work intends to establish a device-level characterization sensitive macromodel that will help to determine the expected polarization of the outputs and how it changes with temperature, at higher levels of design itself. It also establishes the design sensitivity with respect to operational errors.

We demonstrate and validate our model using commonly studied *multiclocked* QCA circuits and elements, whose behaviors are pretty well understood by others. First, we show that the ground state polarization probabilities of the output nodes as well as the intermediate nodes in the macromodel of the QCA logic circuit closely match with those obtained from a full layout level implementation [8] at different temperatures. Second, we demonstrate that both the ground and the next excited (error) state configuration of the macromodel exactly match the corresponding configurations of the detailed layout cells. The mismatch between the ground and the next excited error state configuration can be used to identify weak spots in circuit design at an higher level of abstraction itself.

II. Modeling Theory

In this section, we explain the hierarchical modeling scheme. We focus on two levels: the layout level and the circuit level, where groups of QCA cells, corresponding to a basic logic element, are represented as one macroblock. For both these levels, we will use the graphical probabilistic model called Bayesian Networks[9] to represent the underlying joint probability of the entire set of nodes. Note that probabilistic representation is essential to capture the inherently uncertain nature of the computing with QCAs.

In Fig. 1(a), we show the QCA layout of a NAND gate. Fig 1(b) shows the layout level Bayesian representation. Note that we have 18 random variables representing the state of 18 QCA cells. Fig. 1(c) shows the circuit level abstraction of a NAND gate. The Bayesian representation of circuit level abstraction (as shown in Fig. 1(d)) has fewer cells and is a collection of cells from the layout level.

The nodes of the Bayesian network are quantified by the conditional probabilities. At the layout level, we need to specify

the conditional probability of the state of a cell given the states of parent neighbors, i.e. $P(x|pa(X))$ where $Pa(X)$ are the direct causes of the random variable X or the parents of the node X in the directed graph representation. *We use lowercase to indicate value of a random variable. i.e. $P(x)$ denotes the probability of the event $X = x$ or $P(X = x)$.* We estimate this using the quantum mechanical modeling of QCA cells. At the circuit level, we need to specify the conditional probability of the output states of a macromodel given the states of the inputs, $P(y|Pa(Y))$. These conditional probabilities are estimated from the conditional probabilities in the layout level model of the QCA cells comprising the macromodel, at different temperatures.Inference or computation with Bayesian networks exploits the sparsely connected graph structure.We refer the reader to [9], [10], [8] for details on the inference scheme that we have discussed later in this work.

A. Layout Level Model of Cell Arrangements

To enable us to form macromodels of various cell arrangements, we need to represent the joint state probabilities of a collection of cells at the layout level. It has been shown in [8] how this joint probability can be efficiently represented using Bayesian networks.

As shown in [8] for a given set of possible parent node assignments, the conditional probability values are computed using the Hartree-Fock approximation, applied locally. The conditional probabilities between the parent ($pa(X)$)-child (X) pair is given by

$$\begin{aligned} P(X=0|pa(X)) &= \rho_{00}^{ss}(pa(X), ch^*(X)) \\ P(X=1|pa(X)) &= \rho_{11}^{ss}(pa(X), ch^*(X)) \end{aligned} \quad (1)$$

where ρ_{00}^{ss} and ρ_{11}^{ss} are the probabilities of observing (upon making a measurement) the system in each of the two states and are given by:

$$\rho_{00}^{ss} = \tfrac{1}{2}\left(1 - \tfrac{E}{\Omega}\tanh(\Delta)\right) \quad \rho_{11}^{ss} = \tfrac{1}{2}\left(1 + \tfrac{E}{\Omega}\tanh(\Delta)\right) \quad (2)$$

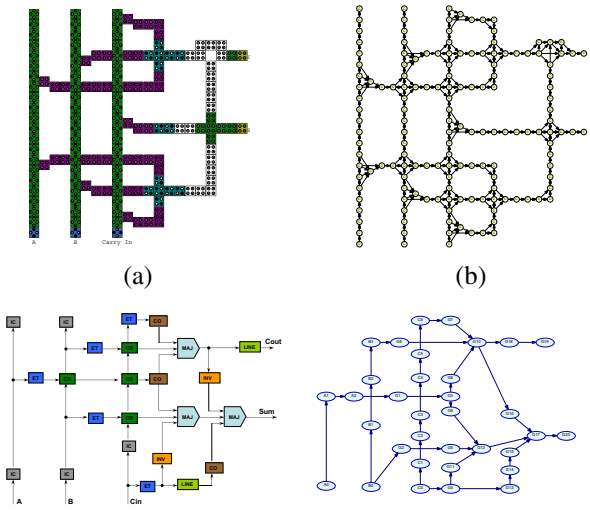
$\Delta = \frac{\Omega}{kT}$ is the thermal ratio k is the Boltzmann's constant and T is the temperature in Kelvin.

Note that once the conditional probabilities between the nodes and its parents are obtained the Bayesian Network is quantified completely.

B. Circuit Level Modeling

The basic circuit elements of a QCA circuit consists of typical logic elements, such as Majority, NAND, AND, OR, and NOT, and QCA specific elements such as wires and crossbars. Table I-B lists all the symbols used for macromodel design blocks that we have used in our designs. The macromodels of different circuit elements are the conditional probability of output cells given the values of the input cells. We compute this by marginalizing over the internal cells. The underlying premise of the macromodeling is that if the joint probability distribution function $P(x_1, \cdots, x_n)$ over all the n cells in the layout is available, using the process outlined in the previous subsection A, then we can always obtain the exact distribution over subset of cells by marginalizing the probabilities over rest of the variables. For instance, the joint probability over just three cells, x_i, x_j, and x_k, can be obtained by

$$P(x_i, x_j, x_k) = \sum_{\forall x_m, m \neq i,j,k} P(x_1, \cdots, x_n) \quad (3)$$



(a) (b) (c) (d)

Fig. 3. A full adder circuit (Adder-2) (a) QCA cell layout (b) Layout level Bayesian network representation. (c) Circuit level representation. (d) Circuit level Bayesian network macromodel.

Hence, at the circuit level, we do not represent all the m internal cells. Note that at circuit level, we only represent $P(x_i, x_j, x_k)$ and represent them with different variable Y, which essentially captures the input-output dependence but is faithful to the layout level quantum interaction since the macromodel is built by marginalizing the layout level cells. This marginalizing is achieved by conducting *average* likelihood inference [9], [10] on the Bayesian network representation over all the cells in the macromodel unit. Note that Eq. 3 will yield different results at different temperatures and we store the conditional probabilities at various temperature points shown in Table I-A. In this table we show a simple majority, clocked majority gate, and inverter. For each macro-cell, we show the QCA layout, layout level Bayesian model, circuit level input-output relation and magnitude of polarization drop with temperature. As it can be seen that polarization drops with increasing temperature and the gradient is dependent on specific input combinations.

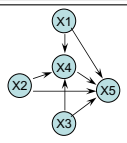
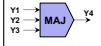
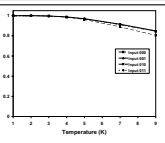
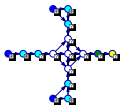
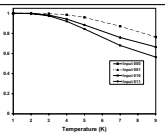
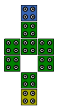
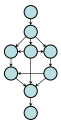
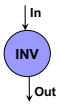
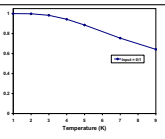
Once we know the logic components required to build a circuit, we simply extract the macromodel logic blocks and the required connectivity blocks (e.g. Line, Corner, Inverter Chain, etc.) from the library at a given temperature and use them to build the logic circuit. We form a Bayesian macromodel using the input-output probabilities of each block. The output from one macromodel block is fed to the input(s) of next macromodel block.

We make two important observations from the circuit level study. First, a clocked majority gate, which is necessary to synchronize all the input signals reaching the majority gate, has weaker polarization at higher temperature compared to the simple majority (Table I-A) as number of cells are higher in the clocked majority gate. Hence if inputs to a majority gate are arriving at the same time, then simple majority yields better polarizations at higher temperatures. Second, inverters have larger drop of polarization over the the majority gates at higher temperatures.

We illustrate the process using a full adder circuit, Adder-2, shown in Fig. 3(a). It consists of five majority gates with no in-

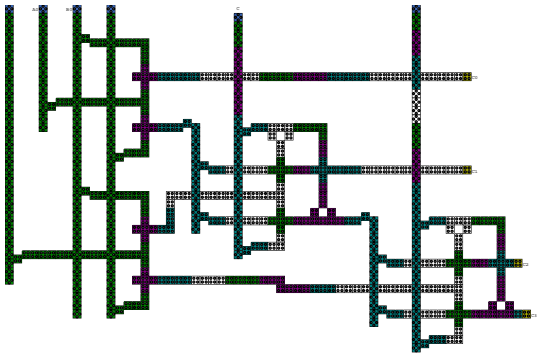
TABLE I

MACROMODEL DESIGN BLOCKS

Macromodel	QCA Layout	Bayesian Model	Block Diagram	Thermal Properties
(a) Simple Majority				
(b) Clocked Majority				
(c) Inverter				

Symbol	Macromodel
Maj	Simple Majority Gate
CM	Clocked Majority Gate
Inv	Inverter
Line	Line Segment
CO	Corner
IC	Inverter Chain
OT	Odd Tap
ET	Even Tap
CB	Crossover
AND	And Gate
OR	Or Gate
ZL	z-line

(A) (B)



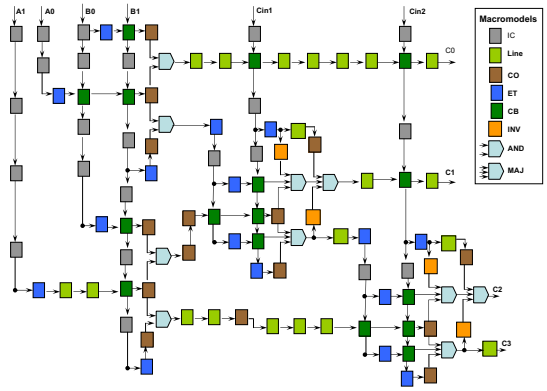


Fig. 2. A QCA 2x2 Multiplier circuit(a) QCA multiplier cell layout (b) Macromodel representation

verters. Fig. 3(b) shows the corresponding layout level Bayesian network. We model the circuit level QCA macromodel shown in Fig. 3(c) which is the circuit level abstraction of Fig. 3(a). The Bayesian macromodel is shown in Fig. 3(d). Each signal (node) can either be a primary input, or an output cell of a macroblock like line, inverter etc. The links are directed from the input to the output of each macroblock and are quantified by the device macromodels. Thus, we arrive at directed acyclic graph easily from the circuit model in Fig. 3(c).

III. ERROR COMPUTATION

Another analysis of interest when comparing designs is the comparison of the least energy state configuration that results in correct output versus those that result in erroneous outputs. What is the probability of the minimum energy configuration that results in *error* at the output, x_s, for a given input assignment, $x_1, \cdots, x_r$? This can be arrived at by conditional maximum likelihood propagation. In essence, we compute $\arg\max_{x_1,x_2,\cdots,x_r} P(x_{r+1}, \cdots, x_N | x_1, \cdots, x_r, x_s)$ and the minimum energy configuration of all the cells that generates the erroneous output x_s is $\{x_1^e, x_2^e, \cdots x_{r+1}^e, \cdots x_N^e\}$. This configuration corresponds to the most likely error state at the output x_s. Whenever we have $x_i^g \neq x_i^e$, the i^{th} cell is considered sensitive to error at output x_s (also termed as weak spots).

This kind of maximum likelihood analysis can be conducted both at the layout and the circuit levels. Let us say that the circuit level macroblocks have $Y_1, \cdots, Y_r$ as inputs and $Y_{r+1}, \cdots, Y_M$ as internal circuit level lines (nodes). Let us say that the ground state macroblock cell polarizations are denoted by $\{y_1^g, y_2^g, \cdots y_{r+1}^g, \cdots y_M^g\}$. With respect to the the erroneous output y_s, let the minimum energy configuration is $\{y_1^e, y_2^e, \cdots y_{r+1}^e, \cdots y_M^e\}$. As in the case of layout, whenever we have $y_j^g \neq y_j^e$, the j-th cell is considered sensitive to error at output y_s.

In the next section, we will presents results that show that the error modes of the circuit and layout levels match. That is, whenever Y_j is sensitive to the first-excited error state for output Y_s, the corresponding layout level model, shows the set of $\{X_i\}$ that constituted the macroblock Y_j is also sensitive.

IV. RESULTS

We present results using a 2x2 multiplier, which is a somewhat larger design than Adders. First, we will show that the ground state polarization probabilities of the output nodes as well as the intermediate nodes in the macromodel of the QCA logic circuit closely match with those obtained from a full layout level implementation [8] at various temperatures. Second, we demonstrate that both the ground and the next excited (error) state configuration of the macromodel exactly match the corresponding configurations of the detailed layout cells for two full adders designs. As we can see from the Table II, the simulation time required to evaluate a circuit is orders of magnitude lower than that in QCADesigner tool [11]. We can see that macromodel is order of magnitude faster which would be important in synthesizing larger networks of QCA cells.

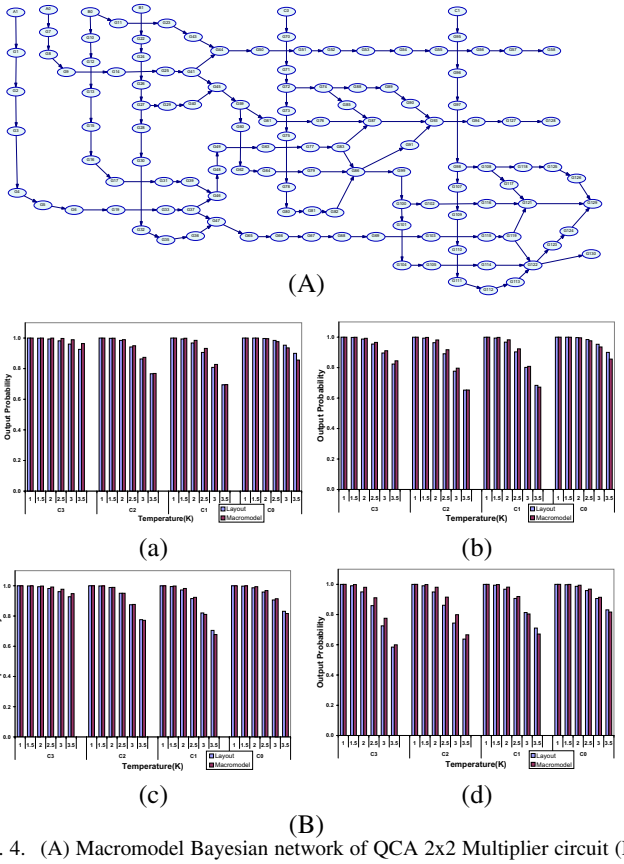


Fig. 4. (A) Macromodel Bayesian network of QCA 2x2 Multiplier circuit (B) Probability of correct output at the four output nodes of 2x2 Multiplier circuit based on the layout-level Bayesian net model and the circuit level macromodel, at different temperatures, for different inputs (a)(1,0),(0,1) (b) (1,0),(1,1) (c) (1,1),(0,1) (d) (1,1),(1,1).

TABLE II

COMPARISON BETWEEN SIMULATION TIME (IN SEC) OF A FULL ADDER AND MULTIPLIER CIRCUIT IN QCADESIGNER(QD) AND GENIE BAYESIAN NETWORK(BN) TOOL FOR FULL LAYOUT AND MACROMODEL LAYOUT

Simulation Time (sec)	Adder-1	Adder-2	2x2 Multiplier
QD Coherence Vector	566	253	966
QD Bistable Approx.	5	3	15
QD Nonlinear Approx.	3.5	2	8
BN Full Layout model	0.240	0.030	0.801
BN Macromodel Layout	0.010	0.000	0.08

A. Polarization

The 2x2 multiplier circuit shown in Fig. 2(a) consists of two AND gates and two half adders. We made use of a half adder similar to Adder-2 full adder design, for the simple reason that it occupies less area. The Bayesian network of the multiplier macromodel design is shown in Fig. 4(A). The polarization of the output nodes in the multiplier layout is almost similar to that obtained at the outputs of multiplier circuit designed using the macromodel blocks as can be see in Fig. 4(B). In that figure we show the variation of output nodes C0,C1,C2 and C3 of the multiplier with respect to temperature for both layout and macromodel design for four different input vector sets. Similar results are obtained for other input vectors too.

B. Error Modes

We compute the near-ground state configurations that results in error in the output carry bit C_{out} of a QCA full using both the layout and circuit level models. These are shown in Fig. 5.

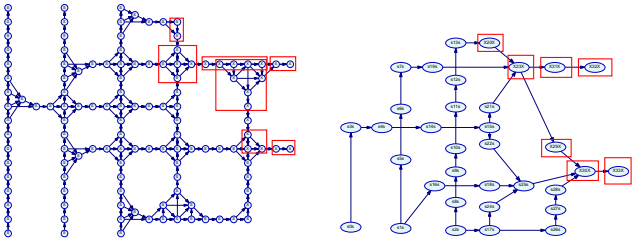


Fig. 5. Error-prone nodes for first-excited state at carry output in a QCA Adder Circuit and its Macromodel design. It can be seen that the erroneous nodes in the layout are effectively mapped in the macromodel design. Input vector set for (a) and (b) is (1,0,0).

We show the case for input vector set (1,0,0). The other input vector sets have similar results. We use red marker to point to the components that are weak (high error probabilities) in both the layout and circuit level. We can easily see that the nodes with high error probabilities in QCA layout are the ones that are clustered to form an erroneous node in the macromodel circuit design. In other words, if a node (a macromodel block) in macromodel circuit layout is highly error prone for a given input set, then some or all the QCA cells forming that macromodel block are highly prone to error. This indicates that weak spot in the design can be identified early in the design process, at the circuit level itself.

V. CONCLUSION

In this work, we illustrate our macromodeling idea using a full adder macro model design and a somewhat larger QCA design of a 2x2 Multiplier. We found that both the polarization and the error mode estimates at the circuit level match those at the layout level. The developed models in this work can be used to selectively identify weak components in a design early in the design process. It would then be possible to reinforce those weak spots in the design using reliability enhancing strategies. The error modes can also be used to compare multiple designs early on in the process.

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