

EEL 3302; ELECTRONICS I

EXAMINATION #2 — 10/24/07

Student _____

(Print Name Clearly)

INSTRUCTIONS

1. This is an open-book open-notes examination to be completed outside class. All necessary worksheets, graphs and tables will be supplied as part of the examination booklet. All examination pages must be submitted for grading. Do not unstaple and separate the examination booklet pages. Put your name on the first page only.
2. Show all work in detail. You must supply sufficient detail to allow Prof. Gordon to follow your work if you want credit.
3. If you require extra workspace to present your solution, use the extra pages included in the examination. Do not write on the back side of any examination page; back sides will not be graded. Clearly identify each problem continuation page. Mark your final answer(s). Failure to comply may result in proportionate credit loss.
4. The solutions that you submit must be solely the product of your own effort. Do not consult other people about anything related to the exam; ask Prof. Gordon if you need clarification about the examination.
5. Indicate your honorable conduct below. Return the signed sheet with your examination.

This work is solely the product of my effort. I have neither given nor received assistance related to this examination, and I have read, understood and complied with the requirements of this examination to the best of my knowledge.

(signature)

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#1) (20 Points)

Analyze the circuit shown in Figure 1 to determine the voltages at all MOSFET connections and the currents through all resistors (6 answers). Let $V_t = 1.4$ V and $k'_n(W/L) = 25$ mA/V². Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a dual 15 V power supply. Show all work in detail.

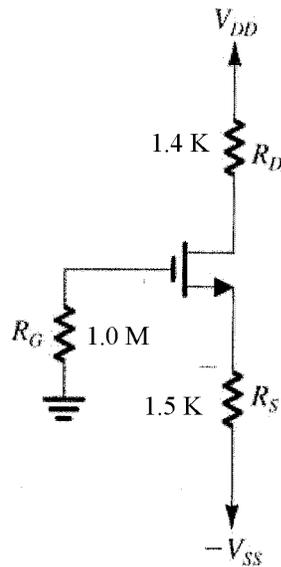


Figure 1 MOSFET Bias Configuration

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#2) (20 Points)

For the circuit shown in Figure 2, determine the values for R_{G1} , R_{G2} , R_S and R_D to provide an operating point at $V_D = 10\text{ V}$, $V_S = 5\text{ V}$ and $I_D = 10\text{ mA}$. Let $V_t = 1.4\text{ V}$ and $k'_n(W/L) = 25\text{ mA/V}^2$. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Show all work in detail.

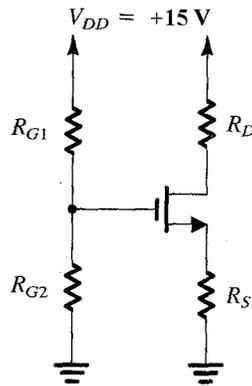


Figure 2 MOSFET Bias Configuration

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#3) (20 Points)

An n-channel enhancement-mode MOSFET operating as a common-source amplifier employs both fixed bias and self-bias. A voltage divider with Thevenin equivalent resistance of 100 Kohms fixes the gate voltage at 7 volts dc using a 20-V supply. The source resistor is chosen to provide a drain current of 10 mA. The drain resistor is chosen to provide a drain-to-source voltage of 10 volts dc using the same 20-volt supply. The MOSFET has $V_t = 1.4 \text{ V}$ and $k'_n(W/L) = 25 \text{ mA/V}^2$. Include the channel-length modulation effect for $\lambda = 0.02 \text{ V}^{-1}$. The amplifier is driven by a source with 200-ohm internal resistance and there is no external load resistance.

- a) Draw the schematic diagram for the amplifier.
- b) Draw the small-signal linear equivalent circuit for the amplifier.
- c) Determine the input resistance, the output resistance and the overall voltage gain.

Show all work in detail.

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#4) (20 Points)

Consider the amplifier shown in Figure 3. The MOSFET is biased at $I = 10$ mA with $V_{GS} = 2.5$ V @ $I_D = 10$ mA, $V_t = 1.5$ V, $C_{GS} = 5$ pF, $C_{GD} = 2$ pf and $V_A = 50$ V. The circuit elements are as follows: $R_{sig} = 50$ Ω , $R_G = 1.0$ M Ω , $R_D = 750$, $R_L = 1.0$ K; $C_S = 100$ μ F, $C_{C1} = 0.1$ μ F, $C_{C2} = 10$ μ F, $V_{DD} = 15$ V dc and $V_{SS} = 15$ V dc.

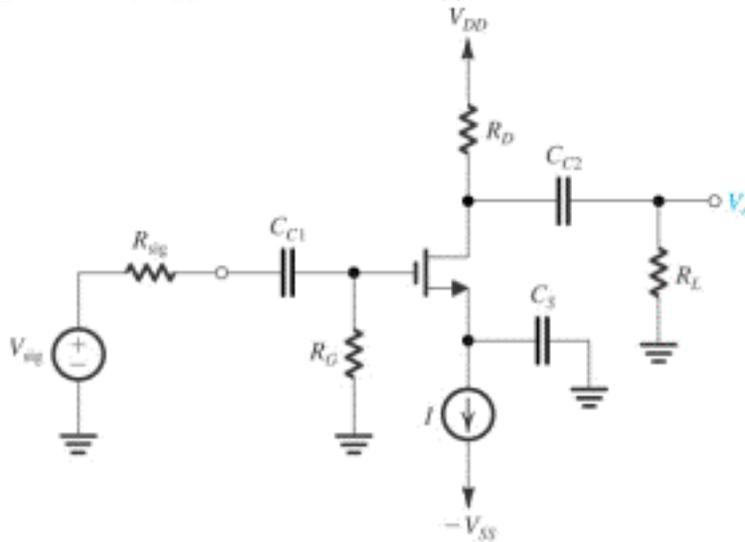


Figure 3 AC-Coupled Common-Source Amplifier

- Determine the overall voltage gain, the input resistance with R_L in place and output resistance with V_{sig} in place but set to supply zero output.
- Determine the cutoff frequencies associated with C_{GS} and C_{GD} , C_{C1} , C_{C2} and C_S (four answers).
- Sketch a plot of the overall voltage gain frequency response. Style your plot on the combination of text Figure 4.50 and text Figure 4.52.

Show all work in detail

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#5) (20 Points)

Figure 4 shows an NPN BJT embedded in a bias arrangement. The BJT dc current gain $\beta_{dc} = 50$ and $V_{BE} = 700 \text{ mV}$.

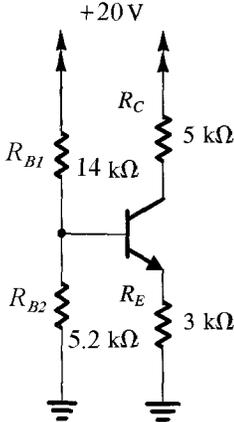


Figure 4 NPN Bipolar Transistor Bias Circuit

Determine the base, emitter and collector voltages and currents (six answers). The dc current gain must be included in your calculations. Show all work in detail.

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Additional Work Space

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