EEL 6936; RF & MICROWAVE CIRCUITS II

CAD EXERCISE #3 (Due 3/5/03)

ANALYSIS OF MICROSTRIP ELEMENT MATCHING CIRCUITS

The purpose of this exercise is to provide an opportunity to become familiar with the simulation and analysis of microstrip element matching networks. Example 2.5.2 from Gonzalez "*Microwave Transistor Amplifiers*" will be used. Familiarity with the material in Prof. Weller's WAMI application notes "ADS *Basics*", "*Simulation of Multiple DUT's Using ADS*", "*Using The Linecalc Program In ADS*", and "*Circuit Design Using Microstrip Lines In ADS*" is a prerequisite. The files are on the course web page: p01-010904.pdf, p02-000926.pdf, p05-000802.pdf, p06-000803.pdf.

PART 1. Simulation Procedure, Design 1 Input Matching Network.

1. Refer to Figure 2.5.14, page 167 of Gonzalez. Use Linecalc to determine the dimensions for the stubline and thruline on a .787mm (31 mil) substrate where ϵ_r=4.7 laminated with 0.035 mm copper cladding. The dielectric loss tangent is 0.02 and the roughness can be considered to be zero. Construct a sub-circuit schematic for the input matching network. See Figure 1.
2. Using the schematic from Cadlab 2, construct a sub-circuit schematic that uses ideal transmission line elements. See Figure 2. Construct a schematic containing the two sub-circuits. See Figure 3. This arrangement will allow comparison of the simulated ideal transmission line performance with the simulated microstrip implementation.
3. Simulate S_{11}, S_{21}, S_{12} and S_{22} for each sub-circuit to obtain the results shown in Figure 4 and Figure 5. Note that the S-parameters for the second sub-circuit will be named S_{33}, S_{43}, S_{34} and S_{44}.
4. Simulate the source admittance (Y_S) and source impedance (Z_S) to obtain the results shown in Figure 6 and Figure 7.

PART 2. Simulation Procedure, Design 1 Output Matching Network.

1. Repeat the Part 1 procedure steps 1, 2 and 3 for the output matching network. In step 4 simulate the load admittance and load impedance in place of the source admittance and source impedance.

PART 3. Write-up.

1. Submit printed copies of your schematics and simulation results. Your name should be included on each page.

2. Verify that the plotted values for Γ_S, Y_S, Z_S, Γ_L, Y_L, and Z_L at 1 GHz agree with the text. You do not need to include markers

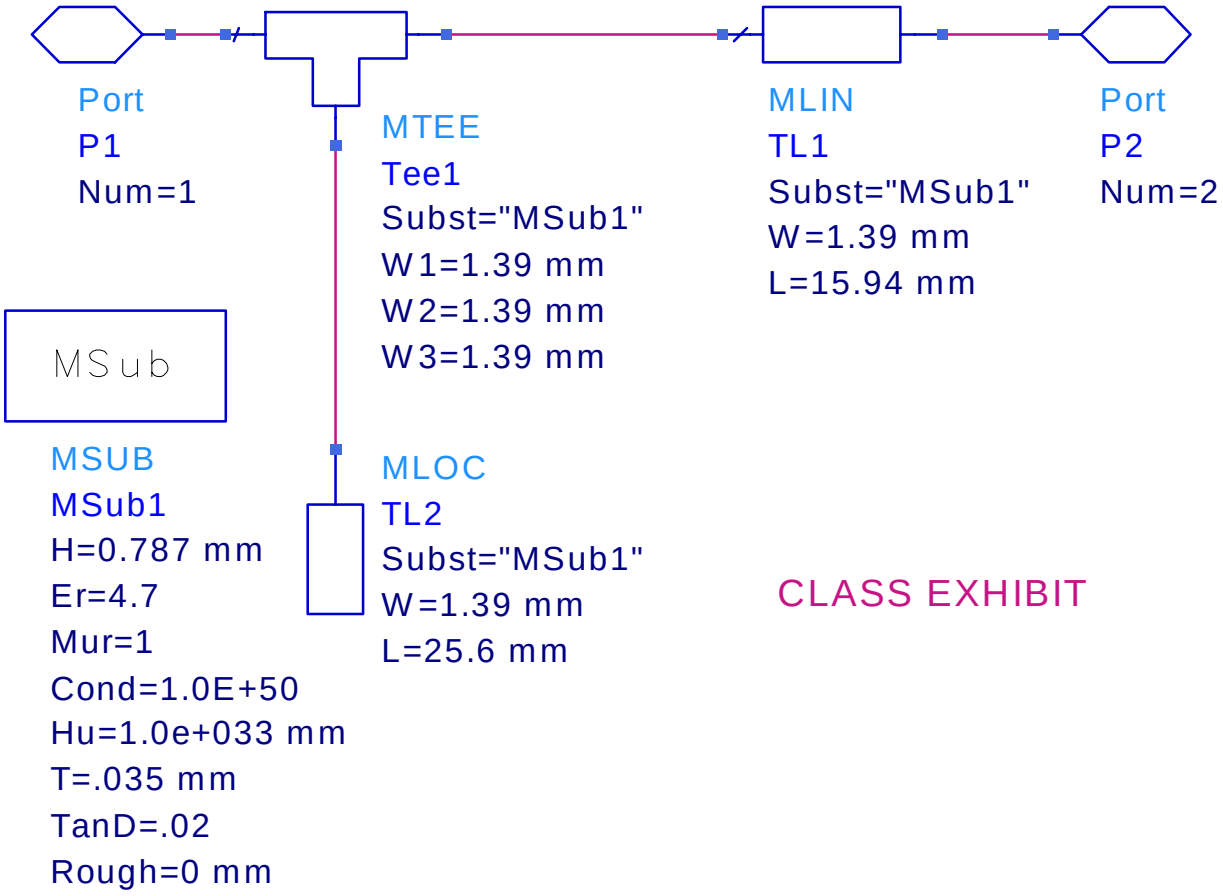
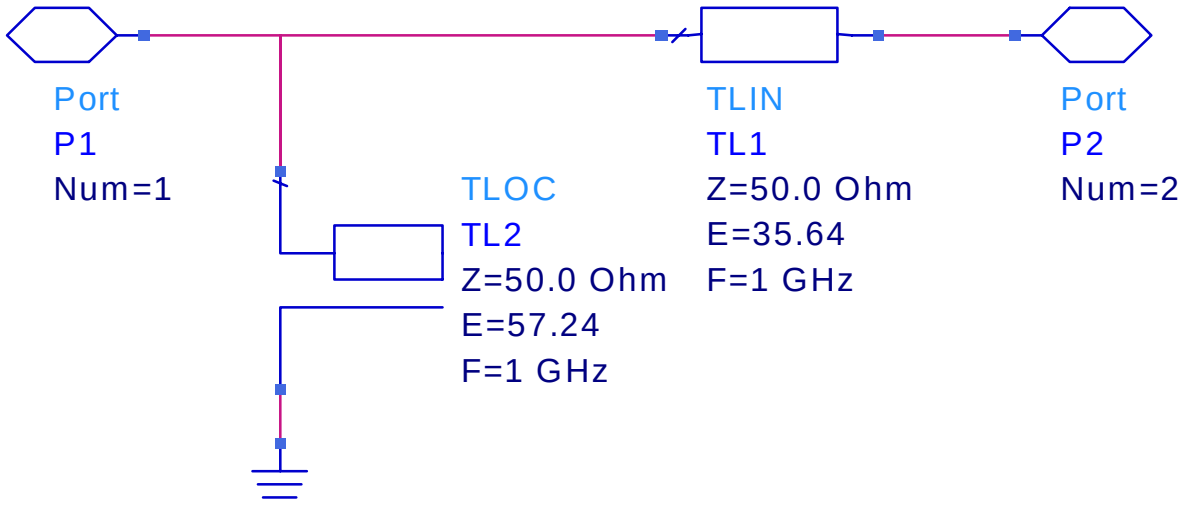


Figure 1. Schematic Diagram For Sub-circuit Using Microstrip Transmission Line Elements.



CLASS EXHIBIT

Figure 2. Schematic Diagram For Sub-circuit Using Ideal Transmission Line Elements.

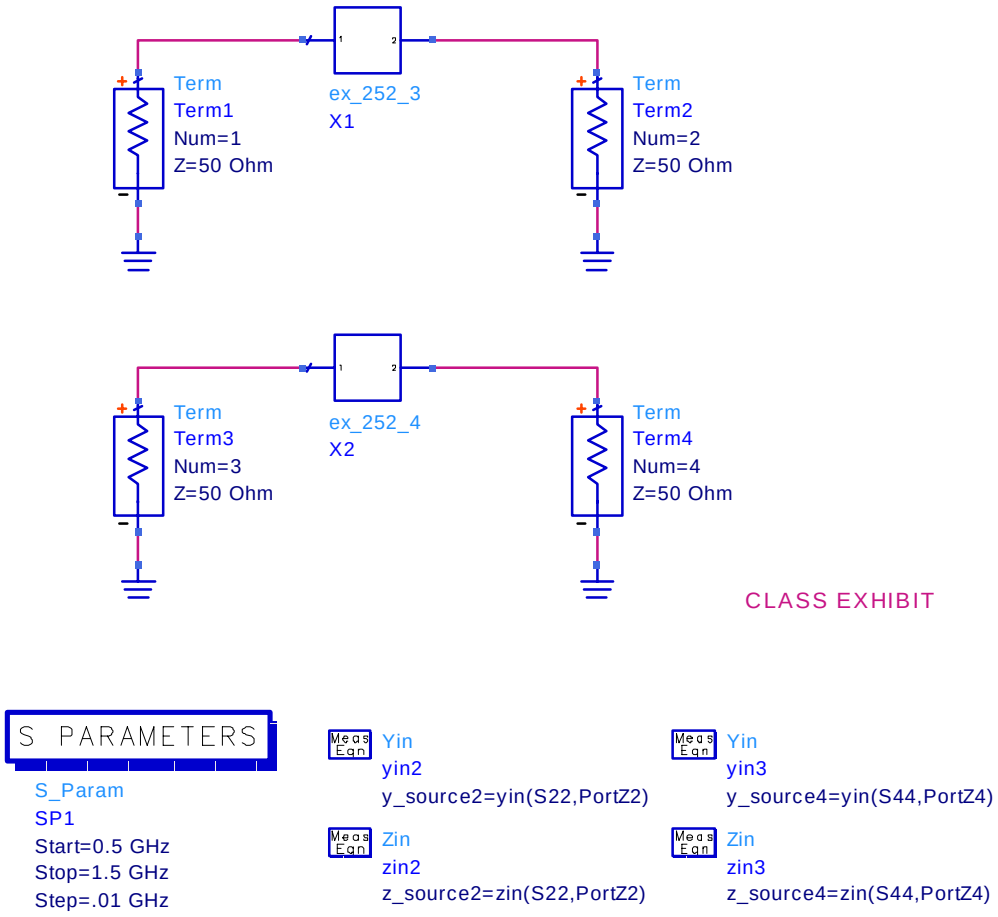


Figure 3. Schematic Diagram For Matching Network Simulation.

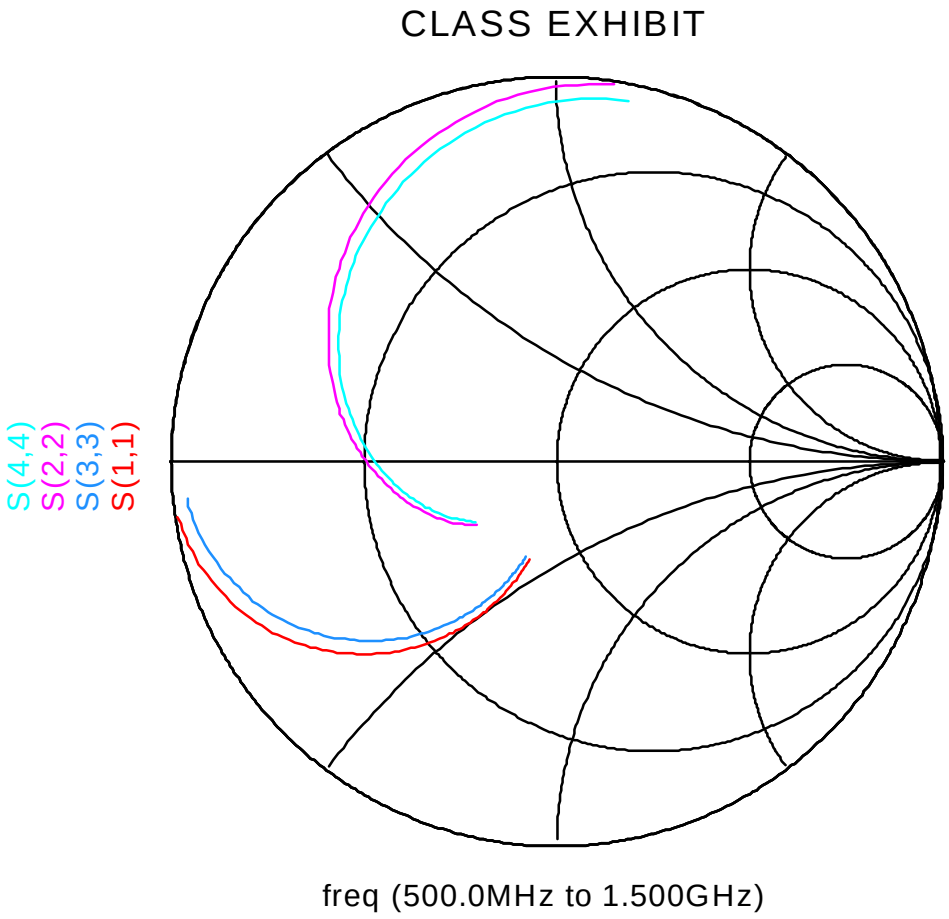


Figure 4. Frequency Response For Γ_s (S_{22}, S_{44}) And S_{11}, S_{33}.

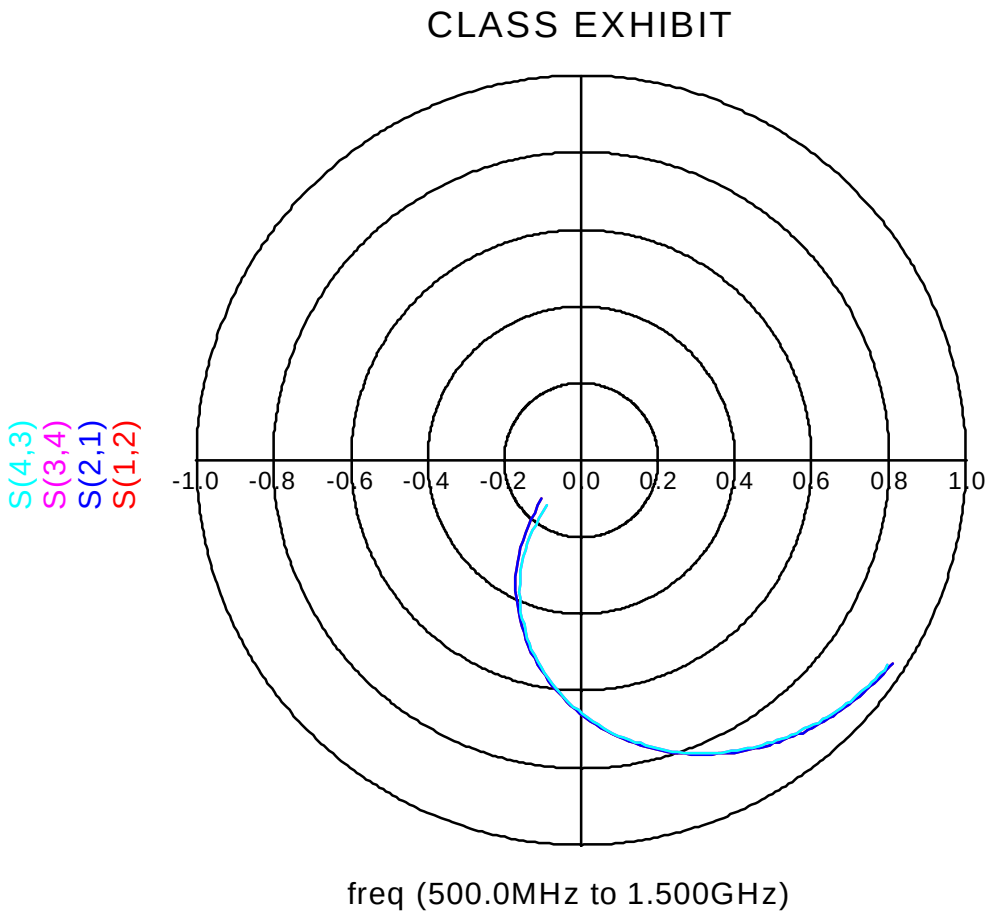


Figure 5. Frequency Response For S_{12}, S_{34} And S_{21}, S_{42}.

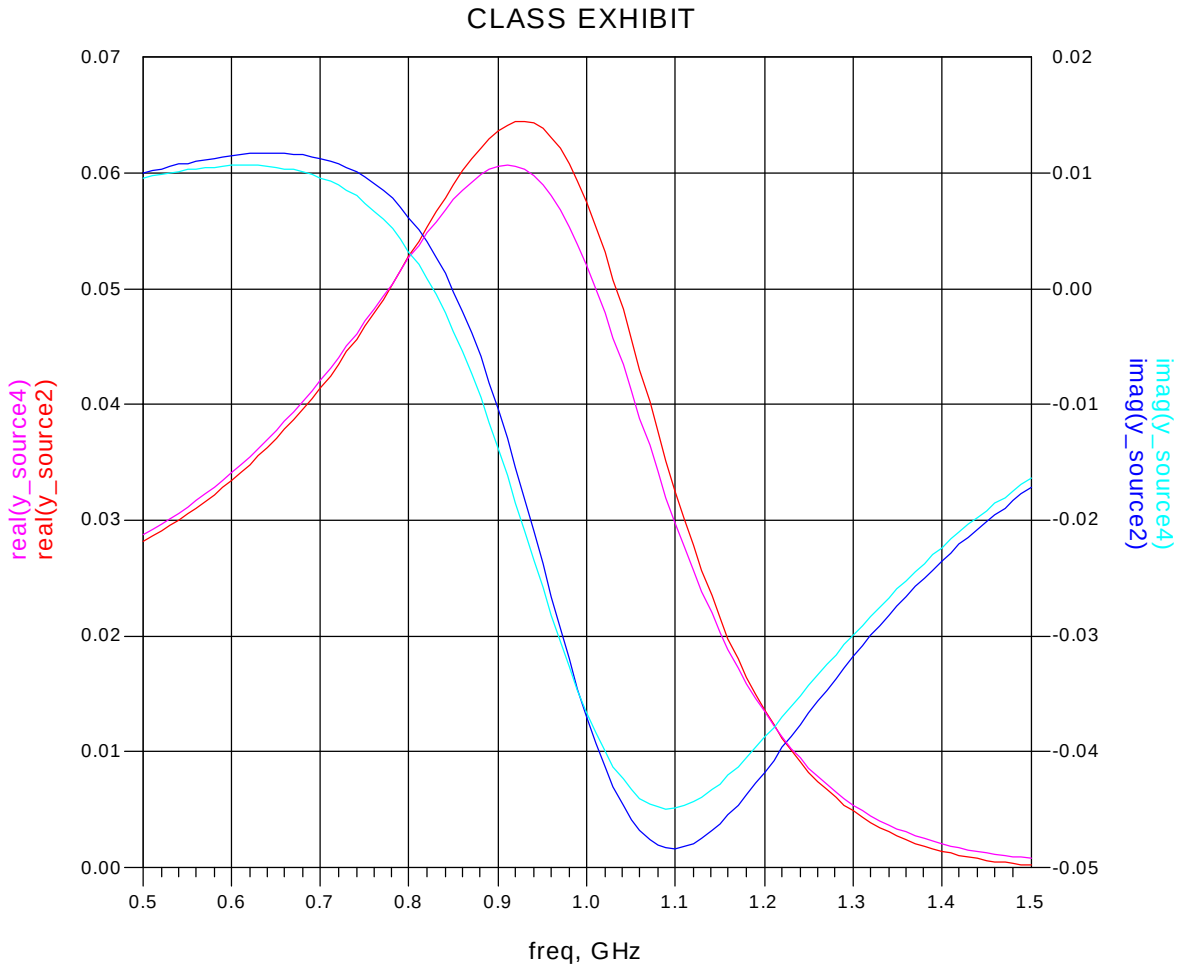


Figure 6. Frequency Response For Y_s.

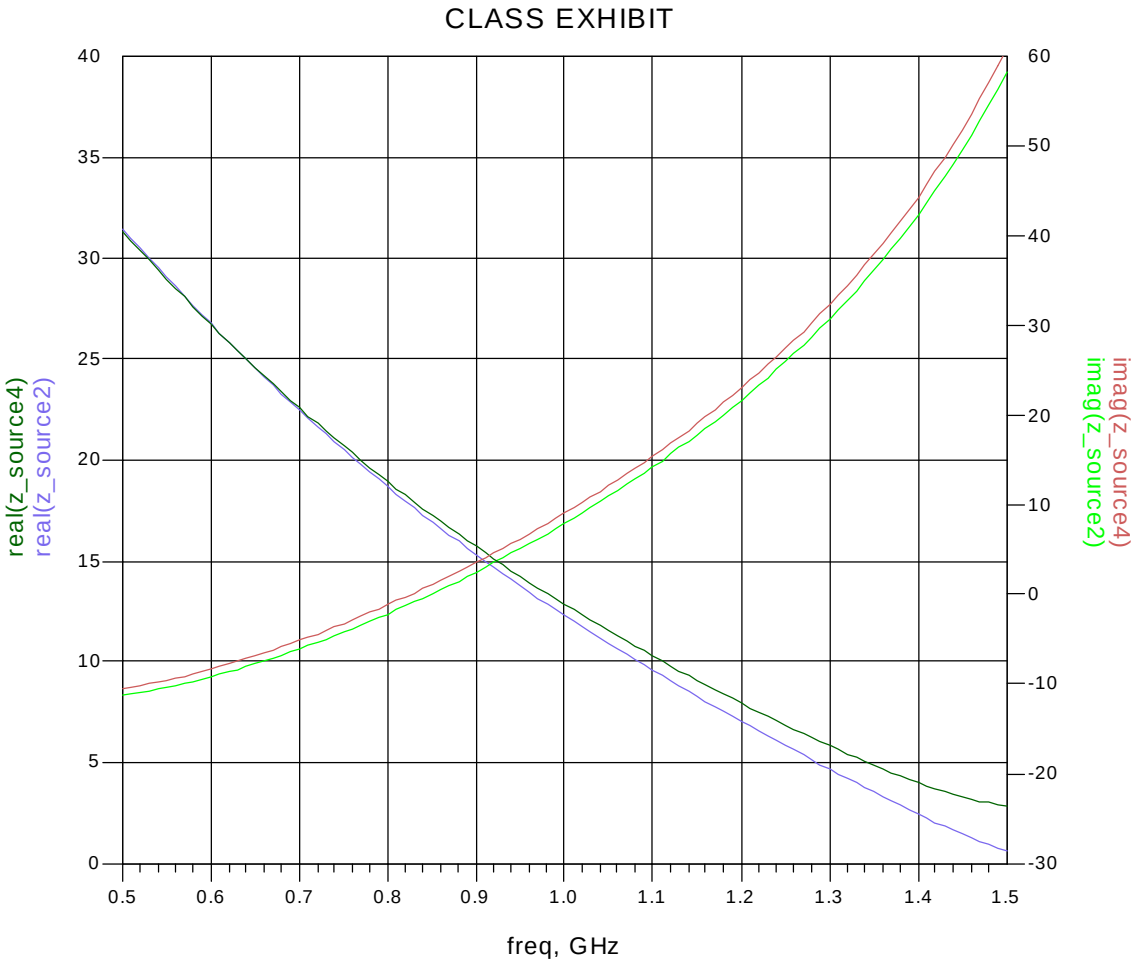


Figure 7. Frequency Response For Z_s.