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Chemical mechanical planarization for microelectronics applications

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Abstract

The progressively decreasing feature size of the circuit components has tremendously increased the need for global surface planarization of the various thin film layers that constitute the integrated circuit (IC). Global planarization, being one of the major solutions to meet the demands of the industry, needs to be achieved following the most efficient polishing procedure. Chemical mechanical polishing (CMP) is the planarization method that has been selected by the semiconductor industry today. CMP, an ancient process used for glass polishing, was adopted first as a microelectronic fabrication process by IBM in the 80 s for SiO_2 polishing. To achieve efficient planarization at miniaturized device dimensions, there is a need for a better understanding of the physics, chemistry and the complex interplay of tribo-mechanical phenomena occurring at the interface of the pad and wafer in presence of the fluid slurry medium. In spite of the fact that CMP research has grown by leaps and bounds, there are some teething problems associated with CMP process such as delamination, microscratches, dishing, erosion, corrosion, inefficient post-CMP clean, etc.; research on which is still developing. The fundamental understanding of the CMP is highly necessary to characterize, optimize and model the process. The CMP process is ready to make a positive impact on 30% of the US$ 135 billion global semiconductor market. This paper presents an overview of CMP process in general, the science and mechanism of polishing, different metal and dielectric CMP processes. The impact of consumables on the CMP process, post-CMP cleaning, modeling of different CMP processes as well as the future trends are also discussed.

Keywords: Chemical mechanical planarization (CMP); Low-*k*; Copper; Polishing pad; Slurry; CMP equipment; Planarization; Tribology; CMP defects; CMP model

1. Introduction

1.1. Generalized semiconductor fabrication processes modules

The relentless competitor and customer driven demand for increased circuit density, functionality and versatility has led to evolutionary and revolutionary advances in the ‘‘front end’’ of the chip manufacturing line where the circuit elements are fabricated, and the ‘‘back end’’ where these elements are appropriately wired within the integrated circuit (IC) [1]. Chip interconnections, or ‘‘interconnects,’’ serve as local and global wiring, connecting circuit elements and distributing power [2]. To incorporate and accommodate the improvements such as decreased feature size, increased device speed and more intricate designs, research in the ‘back end of the line’ (BEOL) processes has

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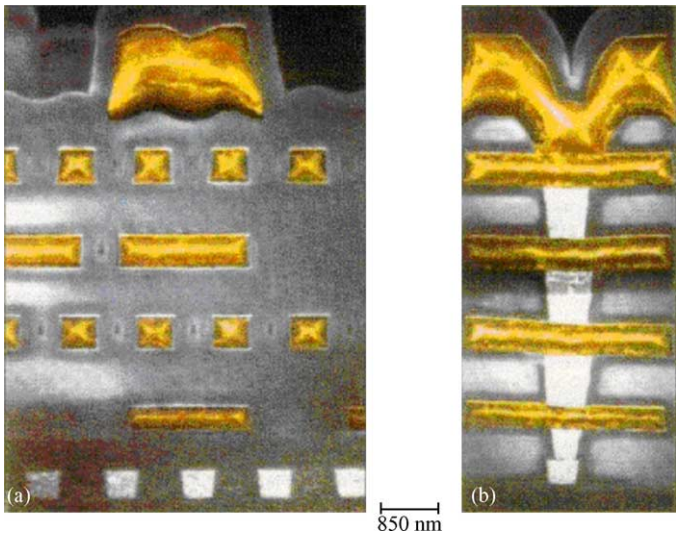

Fig. 1. Scanning electron micrographs of cross-section of the structures fabricated by BEOL technology: (a) BEOL structure of 0.5 μm CMOS logic device and (b) stacked contacts and vias [1,5].

become equally important as the development of the 'front end of line' (FEOL) processes to reduce gate oxide thickness and channel length. Fig. 1(a and b) shows the multilevel interconnect structure which is fabricated using the BEOL processes. The current viable technologies and future trends in scaling bipolar and CMOS transistor fabrication and FEOL technologies have been discussed at length by Taur et al. [3].

1.2. Increase in device density

Over the last 20 years, circuit density has increased by a factor of approximately 10^4 (Fig. 2), while cost has constantly decreased [e.g., the historical 27% per year decline in price per bit for dynamic random access memories (DRAMs)] [3]. The trend is expected to continue in the future even as 65 nm processes are set for production in 2005 [4]. While recent path breaking innovations in the field of lithography and patterning [7–9] have brought about progressive device scaling, the

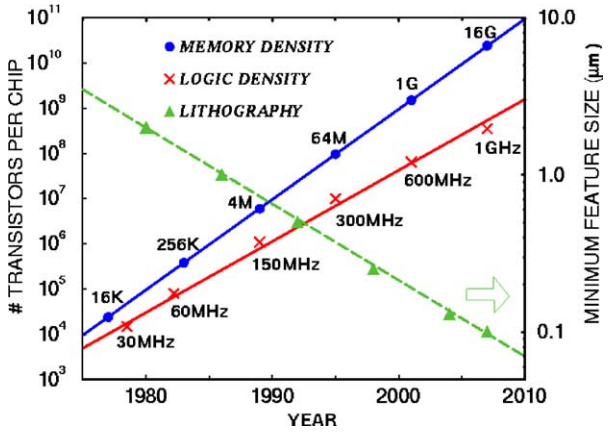

Fig. 2. Trends in logic and memory devices [6].

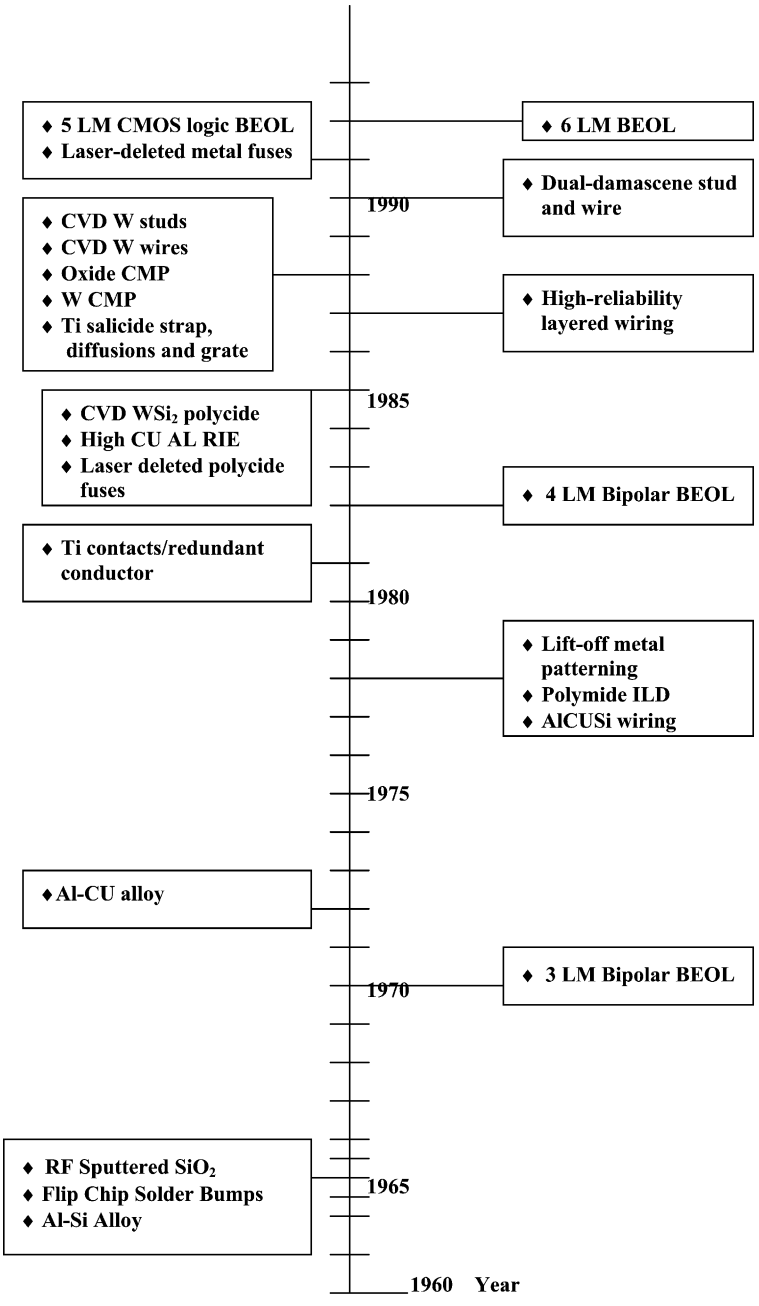

Fig. 3. Chronology of key interconnect technology introduction through the years. LM denotes levels of metallization [1].

development of a planar back-end-of-line approach, which incorporates the use of chemical–mechanical polishing to planarize inter-level dielectrics and metal stud levels, represents a significant advance in BEOL processes. Innovation in BEOL technology is required in each technology generation (Fig. 3), since only part of the density increase could be achieved with improvements in lithography (Fig. 3). The evolution and progressive improvement in the BEOL technology and processes along with the future trends have been elaborately discussed by Ryan et al.

1.3. Scaling and time delay

At the outset, the CMOS device structure had multiple isolated devices connected by single level of interconnect wiring. Scaling down of the device was very effective in achieving the goals of increased device density, functional complexity and performance. However, scaling down of the devices became less profitable, and speed and complexity were dependant on the characteristics of interconnects that wired the devices [10]. With the single level metallization scheme the total area occupied by the wiring on the chip significantly increased with the increase in the active density on the chip. Keyes [11] cited an example of a bipolar chip with a gate count of 1500 gates and a chip area of 0.29 cm^2, fabricated using a single level metal with a pitch of 6.5 μm. The total wiring area occupied by the metal was 0.26 cm^2, which was about 90% of the surface area of the chip.

The total time taken by the voltage at one end of the metal line to reach to 63% of the total value of the step input applied at the other end is known as the interconnect delay and this is due to resistance of the interconnect wiring metal (R) and the interlayer dielectric capacitance (C) [12]. The resistance of the line is given by

$$R = \rho \frac{l}{wd} \tag{1}$$

where ρ is the resistivity of the wiring material, l, w, d, t are the length, width thickness of the wiring material and time for current propagation, respectively. The capacitance of the line is given by

$$C = \varepsilon \frac{wl}{t} \tag{2}$$

The total RC delay can be given by

$$RC = \rho \frac{l}{wd} \varepsilon \frac{wl}{t} = \rho \varepsilon \frac{l^2}{td} \tag{3}$$

Thus, it can be seen from Eq. (3) that RC delay is independent of the line width and further scaling of line width translates in to reduction of IC line thickness which in turn increases the RC delay. Other factors such as parasitic capacitances and cross-talk become dominant for sub 0.5 μm integrated circuits. Apart from incorporating metals of low resistivity, and interlayer dielectrics of lower dielectric constant, forming multilevel metallization schemes where different levels of metal interconnections are isolated by dielectrics and are connected by vertical vias are some of the measures essentially taken to reduce this RC time delay. Table 1 calculates the simple RC time constants calculated for a few metals of given R_s (sheet resistance) and 1 mm length on 1 μm thick SiO_2 [12].

The increasing in the levels of the metallization lines means that packing density need not keep pace with the device density and the minimum metal line feature does not have to scale with the same pace as the gate width. The foremost reason behind the implementation of multilevel metallization schemes is the reduction in the length of the metal lines there by reducing the RC delay sizably (Eq. (3)) and allowing direct routing of the active devices. In places where metal wiring length cannot be reduced, routing can be done at the upper levels without reducing the metal line width thus reducing the RC delay due to the higher surface area. It must be noted that Eq. (3) takes in to account only the line to ground capacitance and does not take in to account the capacitance between adjacent metal lines. The line-to-line capacitance is negligible for wide isolated lines but is significantly large in any sub 3 μm interconnect regime. In sub 0.5 μm the line to line capacitance dominates, there by increasing the RC time delay significantly with scaling. As seen from Fig. 4, there is a dramatic increase in RC time delay in sub 0.5 μm feature size interconnect lines. Starting with two levels of

Table 1
Interconnection delay (*RC*) in silicon VLSI chip

Metal	Bulk resistivity (μΩ cm)	Poly crystalline film resistivity (μΩ cm)	Film thickness (Å)	R_s (Ω/square)	Delay[a] (ps/mm)
Polysilicon	–	~1000	5000	20	690
$CoSi_2$	10	15	2500	0.6	21
$MoSi_2$	~35	~100	2500	4	138
$TaSi_2$	45	55	2500	2.2	76
$TiSi_2$	13	15	2500	0.6	21
WSi_2	~25	70	2500	2.8	97
W	5.65	8–10	2500	0.32–0.4	11–14
Mo	5.2	8–10	2500	0.32–0.4	11–14
Al	2.65	2.7	2500	0.11	4
Cu	1.67	2.0	2500	0.08	3

[a] Delay = RC = 34.5 R_s (ps/mm) for 1 mm length conductor on 1 μm thick SiO_2.

metallization, the levels of metallization have increased up to 8 by 2001 [13]. The future trends in the levels of metallization can be seen in Fig. 5.

The design and layout of interconnect lines is done using the numerous analytical and numerical techniques available. Various techniques have been proposed to investigate the time domain and pulse

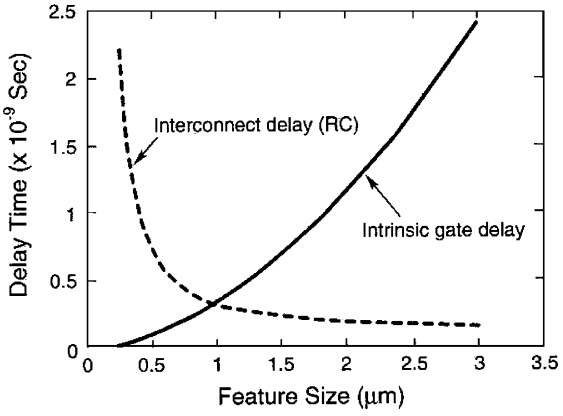

Fig. 4. Total delay vs. minimum feature size [12].

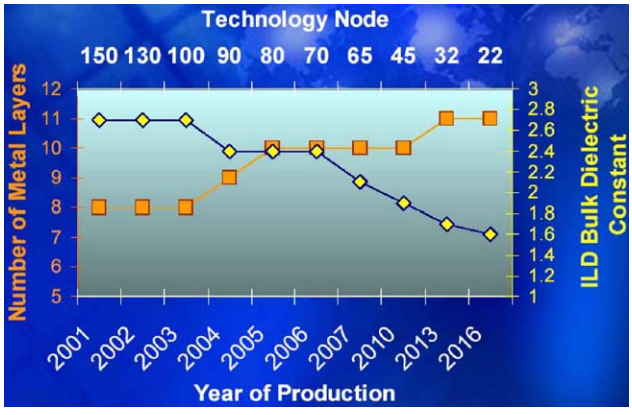

Fig. 5. Future trends in interconnects [13,14].

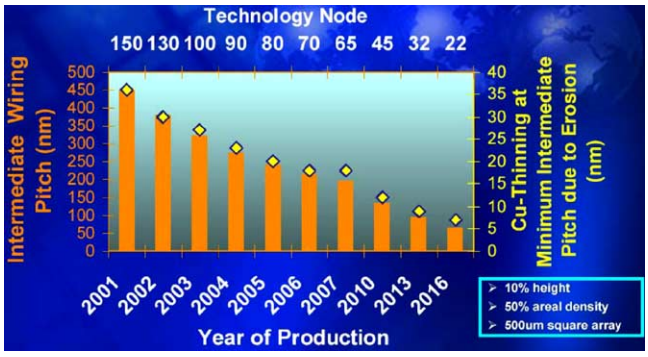

Fig. 6. Chart showing decreases in intermediate interconnect wiring pitch for future generation microelectronic devices [13,14].

propagation characteristics of parallel coupled lossless and lossy lines used to model the interconnect lines in the high speed USLI circuits [15,16]. These techniques include method of characteristics with necessary modifications to incorporate frequency dependant losses [16–18] and congruent modeling techniques where an attempt is made to model the interconnect systems in terms of lumped and distributed circuit elements in computer aided design programs such as SPICE and CADENCE [15,16]. Further details of the design aspects are beyond the scope of this paper.

It is widely accepted that the minimum feature size of the devices on the chip also implies the decrease in the intermediate pitch of the interconnect wring that connects these active devices (Fig. 6) [10].

1.4. Need for planarization

With the decreasing intermediate wiring pitch, non-planarized surface topography results in several processing difficulties. The irregular surface causes a hindrance in conformal coating of the photoresist and efficient pattern transfer with contact lithography. The anomalies in the surface cause the variation of the thickness in fine line widths (sub 0.5 μm) depending upon photo resist thickness. Effectively planarized surface has enormous amount of benefits such as (a) higher photolithography and dry etch yields; (b) elimination of step coverage concerns; (c) minimization of prior level defects; (d) elimination of contact interruption, undesired contacts and electro-migration effects; (e) reduction of high contact resistance and inhomogeneous metallization layer thickness; and (f) limitation in the stacking height of metallization layers. Fig. 7(a and b) shows a comparison between planarized and non-planarized surface topography.

1.5. Shallow trench isolation

Shallow trench isolation (STI) has become a key technology for device isolation in recent times [20,21]. The importance and the need for shallow trench isolation have been discussed by Wolf [22]. The method comprises of making a shallow trench on a silicon wafer, depositing SiO thereon, and then planarizing with a chemical mechanical polishing (CMP) process. The method can separate elements within a much narrower area, and shows much better performance than the conventional local oxidation of silicon (LOCOS) method, which causes bird's beak structures [23].

The details of fabrication of STI structures have been elaborately given discussed Jeong et al. [24]. Until now, a complicated reverse moat etch process had to be used in the absence of sufficiently selective slurries for SiO to SiN polishing. Using an etch process, the high-density moat regions can be

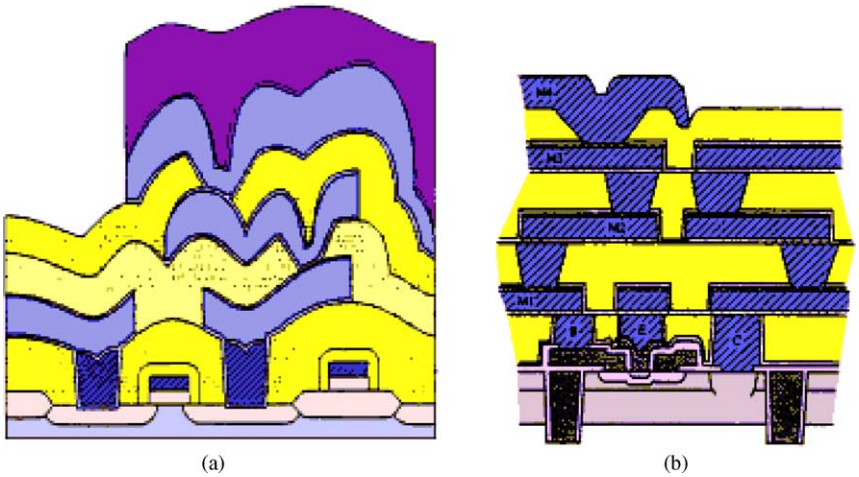

Fig. 7. (a) Schematic of a non-planarized and (b) planarized MLM structure [19].

reduced to an acceptable level, and therefore the chip or wafer level polishing uniformity can be greatly enhanced. If direct CMP without the reverse moat etch process was applied with conventional low selectivity slurries, damage might occur to active regions in the case of excessive CMP, whereas, in the case of insufficient CMP, nitride residues might remain in the active regions after the nitride strip process due to oxide residues [20–25]. The schematic representation of the STI structure fabrication reported by Kim and Seo is shown in Fig. 8 [26].

The process of fabrication of STI structures is still under considerable research [29–30]. One of the main areas of interest is development of silica and ceria-based high selectivity slurries (HSS) [24] with a high polishing selectivity for silicon oxide and silicon nitride [25,26]. There is considerable research currently underway in the STI–CMP aspects such as effective and in situ end point detection

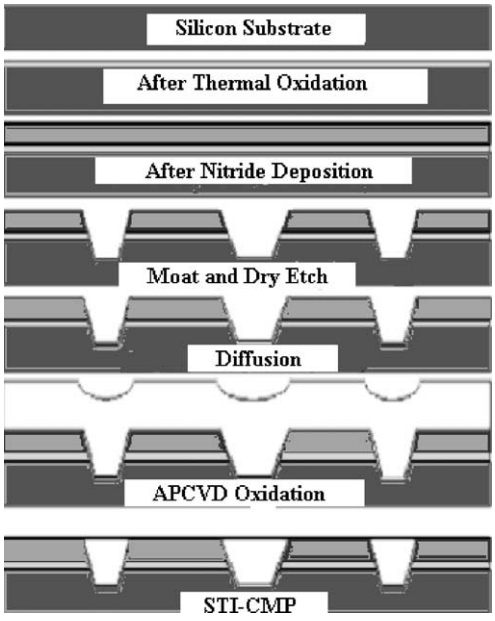

Fig. 8. Schematic of a processes sequence of direct STI CMP without reverse moat [25].

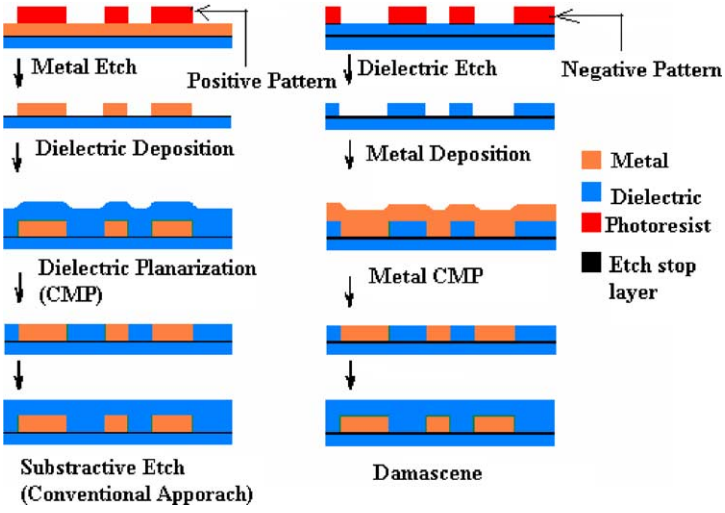

Fig. 9. Comparison between the subtractive etch (conventional approach) and the damascene approach for metallization.

[20–25], reproducibility [24], defect analysis [27,28], pattern density effects [26], etc. The STI CMP process has also been extensively modeled [31–33].

1.6. Damascene process

As seen in Fig. 9, in the conventional metallization technique, the metal deposited on top of the dielectric is positively patterned with photoresist. The metal is then etched out and dielectric material is deposited on top of the metal using processes such spin coating or chemical vapor deposition (CVD) [34]. The dielectric is then planarized and subsequently to make a multilevel metallization structure, more dielectric is deposited on top of the planar dielectric and the process is repeated. In case of the damascene process, the dielectric is negatively patterned, and then etched to form a pattern that is then filled with metal. A seed layer of metal is deposited using physical vapor deposition (PVD). Depending upon the metal, a barrier layer of metal is deposited before the seed layer deposition [35]. The metal is then electroplated on top of the seed layer. The excessive metal is polished off and planarized using the CMP process. For the purpose of making multilevel metallization structures, dielectric is then spin coated or CVD deposited and entire procedure is repeated.

In actual damascene process, a variety of integration sequences can be and need to be applied in order to etch vias and lines into the inter-level dielectric (ILD) [36]. The due considerations need to be given to via tapering [36] and ease of lithography. The integration of low-k materials into dual damascene processes is challenging due to the variety of boundary conditions such as compatibility with metal CMP, metal fill, resist strip and dielectric RIE. Using a PE-CVD SiO_2 cap on top of hydrogen silsesquioxane (HSQ) spin on glass as an ILD solves integration issues related to CMP, resist strip and mechanical stability. The details of Cu and low-k material implementation in dual damascene structure have been discussed in Section 4.

1.7. Different planarization techniques

Fig. 10 shows the different degrees of global and local surface planarity [37]. Techniques such a spin on deposition (SOD), reflow of boron phosphorous silicate glass (BPSG), spin etch planarization (SEP), reactive ion etching and etch back (RIE EB), SOD + EB have been discussed in this section.

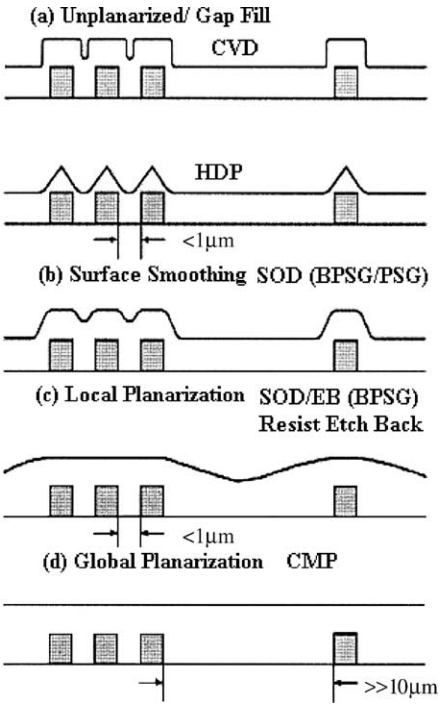

Fig. 10. Different degrees of planarity [37].

These are the prominent of several competing technologies presently being used to achieve local and global planarization.

1.7.1. Doped glass reflow

Synthesis of low pressure chemical vapor deposited (LPCVD) boron and phosphorous doped silicon oxide was one of the first planarization techniques in the IC industry used to fabricate the first layer of dielectric (pre metal dielectric) due to its excellent planarization and gettering properties [38–42]. By doping SiO_2 with boron and phosphorous, the film boro-phosphate–silicate glass (BPSG) has better smoothing of step corners and it can be made to reflow at high temperature (850–959 °C).

Kobayashi and co-workers [38–42] have given the details of formation of doped BPSG using n-type lightly doped Si wafers. Dielectric glass layers were deposited on the wafers in a (LP-CVD) reactor equipped with $Si(OC_2H_5)_4$, $B(OCH_3)_3$ and PH_3 gas sources and O_2 and N_2 carrier gases. As the reflow characteristics are mainly controlled by viscosity, which in turn is a function of glass chemical bonding [41,42] and structure [42], less viscous, non-crystallized glasses are ideally used for reflow and planarization. These glasses are therefore deposited by LPCVD technique, as they are amorphous, more fluid, have low connectivity and have a released structure.

1.7.2. Hydrophobicity

Even though, LPCVD highly boron-containing glasses with low polarizability are favorable for the device planarization in DRAMs and static random access memory (SRAMs) cells, these glasses can be used only for the first level of ILD. This is due to the fact that even the low temperature reflow glasses would melt the metal once deposited as the standard temperature of reflow far exceeds melting point of aluminum. Moreover, high temperatures are unsuitable for other metals due to diffusion and electro-migration issues. Also, due to void formation (Fig. 11) during reflow, and very high thermal budget, the process of doped glass reflow is not a very widely implemented process of planarization.

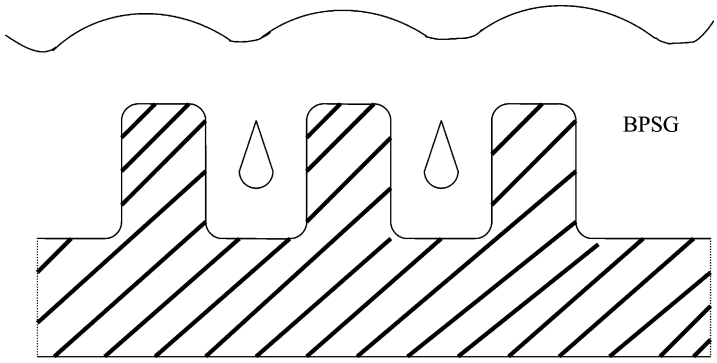

Fig. 11. BPSG void formation after reflow [37].

1.7.3. Spin etch planarization (SEP)

The process of CMP gained increasing prominence due to controlled chemical etching of some metals like Cu was not a very feasible task. However, spin etch planarization, a process developed by Levert et al. at SEZ America Inc. [43] is based on the principles of controlled chemical etching of metals. During SEP, the wafer is suspended horizontally on a nitrogen cushion above a rotating chuck (Fig. 12). The substrate is held in place laterally with locking pins on the wafer edge. As the chuck and wafer are spun, wet etch chemistries are dispensed onto the wafer. A planar final surface is achieved by using an appropriate etching solution and the spinning of the wafer while removing the excess copper. Deionized water and nitrogen are then applied onto the wafer to achieve rapid cleaning and dry-in/dry-out-processing. Results show that the etch rates can be as high as 14,000 Å/min. 200 mm electroplated wafers can be planarized with appropriate chemistries and processing parameters [43].

As there is no contact of any external body with the wafer surface, there is no possibility of typical CMP defects like micro scratches, delamination, peel off, etc. There is reduced instance of dielectric dishing and erosion of metal lines and with in wafer non-uniformity is kept as low as 9.2%. Even though this process has some distinct advantages over CMP, this being a totally new process, is yet to be applied in the industry. The process is expected to increase the cost of ownership (CoO), has not

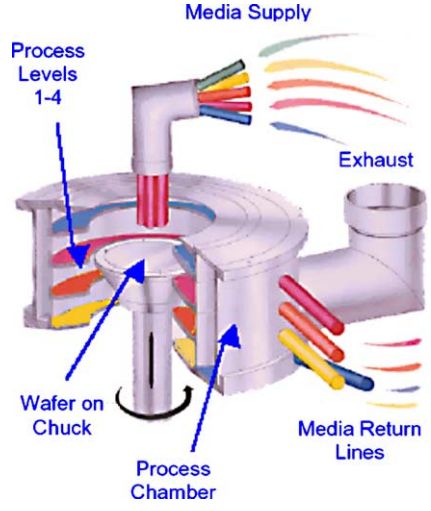

Fig. 12. Schematic of SEP chamber showing a cut-away view of the process pot, four chambers and chuck. The chemical dispense arm, drain lines and exhaust ports also are indicated [43].

been demonstrated on any other materials such as ceramics and insulators. The pattern dependence and etch anisotropy are yet to be further investigated. CMP may be still needed after SEP process to remove pattern dependent bumps on the surface of the wafer. Efficient end point detection mechanisms, in addition to the optical end point detection mentioned by Levert et al. have to be developed for the process. Therefore, for implementation of the SEP further studies, characterization and optimization is necessary.

1.7.4. Spin on deposition (SOD)

Porous low-*k* dielectrics, different glasses such as OSG, TEOS used as dielectric materials and polymeric ILD are typically deposited using spin on technique. The precursor solution for the material to be deposited is prepared mostly at room temperature by mixing the base catalyst and suitable organic additives. The wafer surface is pretreated to promote effective sol spreading, followed by dripping the sol on the spinning wafer. Small amount of sol is dripped on wafers that are then rinsed, spun dried, baked and later cured.

SOD demonstrates excellent gap filling capabilities but shows very poor global planarization. Spin on deposited hydrogen silsesquioxane (HSQ) (dielectric constant $k = 3.0$), has been reported to be successfully integrated into devices with five levels of Al interconnect [44,45] and silicon di oxide formed on surface of silicon using silicic acid solution by spin technology [46], has shown relatively good local planarization [47] and is known to have a positive impact on the global planarization of the ILD achieved by CMP.

Numerous defects are known to arise in the spin on deposited materials. There is non-homogeneity in the value of the dielectric constant of these materials with the exposure to plasma in subsequent processing [48]. The spin-on materials also have a tendency to absorb moisture and then release it in the air during the thermal processes. This induces undue stresses in the SOD films there by causing defects such as cracking, shrinking, peel off, degradation, contamination of interconnects and poor thermal stability [49]. For this purpose, techniques such as laser curing need to be implemented to prevent stresses from building into the dielectric film [50]. Thus in spite of the fact that SOD materials show excellent local planarization, blanket SOD materials are not implemented in the industry. SOD materials are implemented only as layers sandwiched between two oxide layers.

1.7.5. Reactive ion etch and etch back

A competing technology for SOD oxide planarization and reflow is the reactive ion etch and etch back (RIE + EB). The technique of reactive ion etching, conventionally used to pattern the thin film on a substrate in this case is used for planarization. The pattern is spin coated with photoresist. The resists fills the trenches and vias of the pattern leaving the hills and mounts on the pattern exposed to the reactive species in the plasma. Typically RIE + EB is used to etch SiO_2 and other dielectrics. Although wet etching is well developed for etching SiO_2, it has inherent limitations due to undercutting of the mask materials, especially for sub micron pattern sizes. A dry etching technique, like RIE + EB, on the other hand, can generate anisotropic etch profiles and for this reason has come into favor. The mechanism of material removal is more due to chemical reaction than due to physical sputtering, although the two mechanisms are synergistic; i.e. the bombardment catalyzes the surface chemical reactions. This leads to anisotropic etching due to the directional nature of the bombardment catalyzed surface chemical reactions [51–54], as well as by physical sputtering. In general, the rate controlling mechanism of etching by the RIE process may be due to physical effects (as in sputtering with inert ions), or chemical phenomena in the sense that the ion bombardment enhances surface chemical reactions with the reactants yielding highly volatile reaction products.

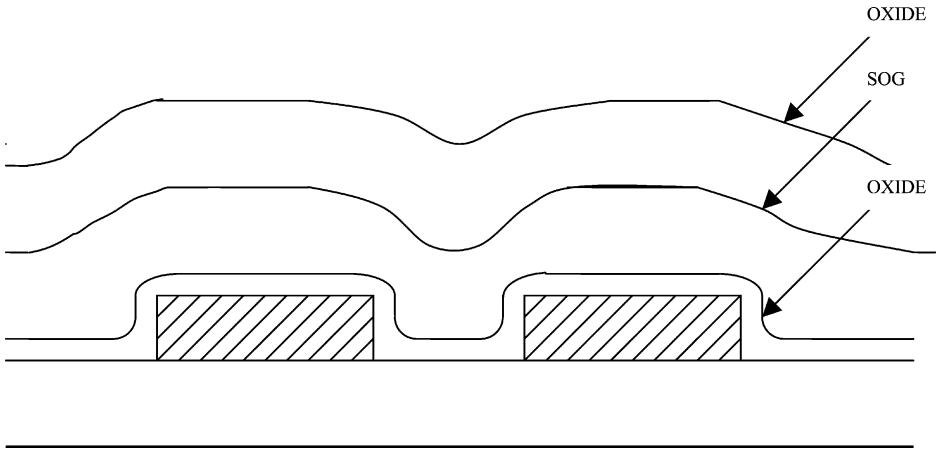

Fig. 13. Spin on deposition local planarization [37].

Fig. 13 shows a schematic of surface smoothening and partial planarization of dielectric with RIE and EB using high-density plasma (HDP) processing. Though RIE is a highly selective process and can be used to etch multiple layers of dielectric or metal, the process needs to be highly optimized in order to avoid small spikes and anomalies on the surface. The artifacts of lithography process can also have an impact on the surface of the wafer. There might be a need for subsequent planarization in order to reduce the surface roughness after etching. The RIE process involves high-energy ion bombardment on the surface of the wafer. This can be extremely dangerous for the device itself and can lead to failure and reliability problems. Though excellent local planarization may be achieved using RIE EB, achievement of global planarization for multilevel thin film structures is still perceived as a problem using RIE EB.

1.7.6. Spin on deposition and etch back

Due to the inadequacies of different planarization techniques, the combination of the two techniques has been used in order to compliment each other, with some degree of success. SOD with Etch back has proved particularly useful in this respect. As the spin on deposited glass has the ability to fill voids and gaps permanently, the technique was developed along with the development of the RIE EB technique. With the emergence of the new spin on polymeric low-*k* dielectrics [51] and other novel spin on materials, techniques like SOD and EB have been pursued with some degree of success in achievement of local planarization on the surface of the wafer. The SOD materials are used to fill the trenches and vias and then RIE process is used to etch back or sacrifice the materials on the higher regions. Subsequently the same material might be deposited using spin on or CVD process to get considerable degree of local planarization. This kind of process is prevalent in gap filling of memory devices (Fig. 14).

Even though the usage of both SOD and RIE EB processes together tend to overcome the drawbacks of each of the processes, the extensive optimization is required for the two processes to work in tandem there by giving good surface planarity. Fig. 15 shows the cross-section of a device structure planarized using SOD RIE EB process.

1.7.7. Chemical mechanical planarization

Presently, CMP is the only technique that can offer excellent local and global planarity on the surface of the wafer. CMP has known to yield local planarization of features as far as 30 μm apart as

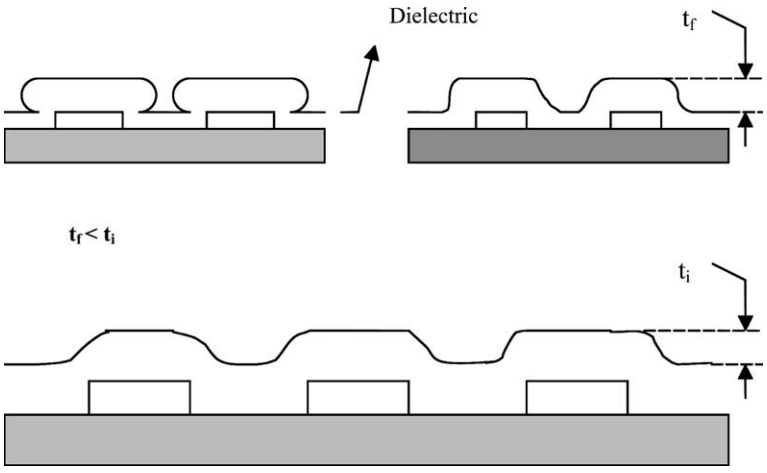

Fig. 14. Smoothening and partial planarization [37].

well as excellent global planarization. The plasma enhanced chemical vapor deposited oxides have limited capability of gap filling and are restricted in their gap filling ability below patterns having 0.3-μm feature size. High-density plasma deposited oxides have acceptable gap filling capabilities; however, they produce variation in surface topography or local as well as global level. Even though spin on deposited (SOD) doped and undoped oxides and polymeric materials have acceptable ability for gap filling, CMP is the only technique, which produces excellent local and global planarity of these materials. The details and various aspects of CMP are discussed subsequently in different sections of this paper.

1.8. Advantages of chemical mechanical planarization

The advantages of chemical mechanical planarization (CMP) are shown in Table 2.

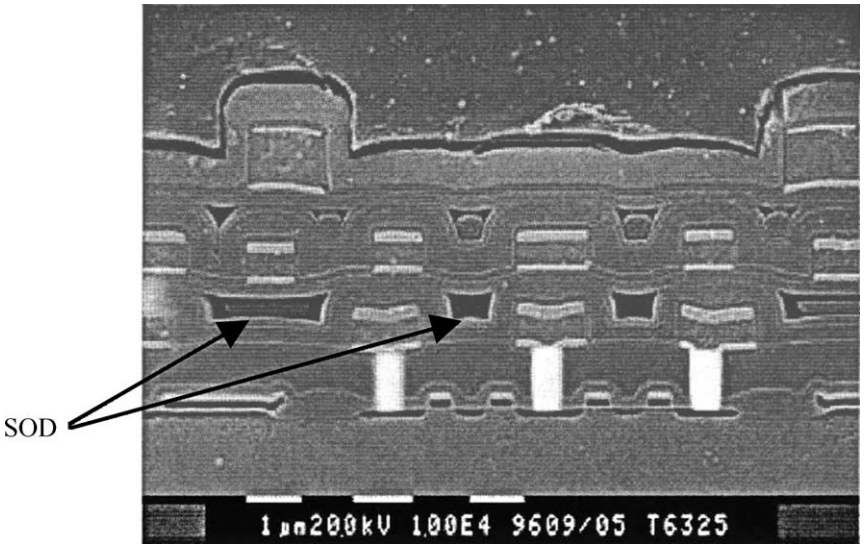

Fig. 15. Cross-section of structure planarized by SOD RIE EB [37].

Table 2
Benefits of CMP

Benefits	Remarks
Planarization	Achieves global planarization
Planarize different materials	Wide range of wafer surfaces can be planarized
Planarize multimaterial surfaces	Useful for planarizing multiple materials during the same polish step
Reduce severe topography	Reduces severe topography to allow fabrication with tighter design rules an additional interconnection levels
Alternative method of metal patterning	Provides an alternate means of patterning metal, eliminating the need to plasma etch, difficult to etch metals and alloys
Improved metal step coverage	Improves metal step coverage due to reduction in topography
Increased IC reliability	Contributes to increasing IC reliability, speed, yield (lower defect density) of sub 0.5 μm and circuits
Reduce defects	CMP is a subtractive process and can remove surface defects
No hazardous gases	Does a not use hazardous gas common in dry etch process

1.9. Drawbacks of chemical mechanical planarization

The disadvantages of chemical mechanical planarization have been tabulated in Table 3.

1.10. General CMP applications

The process of CMP was initially developed and implemented for planarization of SiO_2 which is used as interlayer dielectric in multilevel metallization scheme. The initial developmental focus of CMP was oxide planarization [55]. Tungsten is used as an interconnect plug to the source, drain, and gates of transistors in Si microprocessor chips. Initially Ti and TiN barrier layers are deposited, followed by chemical vapor deposition of W to fill the contact vias. Going ahead from achieving local and global planarization of SiO_2, removal of excessive tungsten from the horizontal surfaces on the wafer pattern proved to be an asset for subsequent Al metallization [56–58]. Hence CMP was developed with a two-fold approach of (1) planarizing oxide and (2) removing the via fill metal from the horizontal surfaces. The major applications of CMP are given in Table 4.

Along with its successful implementation for the achievement of the above-mentioned objectives, CMP has now extended to (a) polishing of different metals like Al, Cu, Pt, Au, Ti, Ta, etc.; (b) polishing of different insulators like SiO_2, Si_3N_4, various low-*k* dielectrics, doped and undoped oxides of silicon; (c) polysilicon; (d) ceramics like SiC, TiN, TaN, etc.; (e) multichip modules; (f) packaging;

Table 3
Disadvantages of CMP

Disadvantages	Remarks
New technology	CMP is a new technology for wafer planarization. There is relatively poor control over the process variables with narrow process latitude
New defects	New types of defects from CMP can affect die yield. These defects become more critical for sub-0.25 μm feature sizes
Need for additional process development	CMP requires additional process development for process control and metrology. An example is the endpoint of CMP is difficult to control for desired thickness
Cost of ownership is high	CMP is expensive to operate because of costly equipment and consumables. CMP processes materials require high maintenance and frequent replacements of chemicals and parts

Table 4
Applications of chemical mechanical polishing [56]

Materials	Application
Metal	
Al	Interconnection
Cu	Interconnection
Ta	Diffusion barrier/adhesion promoter
Ti	Diffusion barrier/adhesion promoter
TiN, TiN_xC_y	Diffusion barrier/adhesion promoter
W	Interconnection e-emitter
Dielectric	
Cu-alloys	Interconnection
Al-alloys	Interconnection
Polysilicon	Gate/interconnect
SiO_2	ILD
BPSG	ILD
PSG	ILD
Polymers	ILD
Si_3N_4 or SiO_xN_y	Passivation layer, hard mask
Other	
Aerogels	ILD
ITO	Flat panel
High k dielectrics	Packaging
High T_c superconductors	Interconnection/packaging
Optoelectronic materials	Optoelectronics
Plastics, ceramics	Packaging
Silicon on insulator (SOI)	Advanced device/circuits

(g) optoelectronic components; (f) flat panel displays; (h) microelectromechanical systems (MEMS); (i) magnetic recording heads and CD read write drives [56].

1.11. Overview

The paper begins with the need for device scaling and implementation of novel materials in the present day semiconductor industry. The importance of planarization and the various available planarization techniques with emphasis on CMP have been discussed in Section 1. Section 2 gives an overview of the CMP process in general and gives the background of the process and equipment used to carry out the process. The different types of equipment used for CMP process and innovations there in have been discussed in this section. The CMP consumables like polishing pad, slurry, retaining rings, etc. have been discussed in Section 3. The novel slurry types such as particle less slurry and nanoparticle slurry and new improvements in the polishing pads have been dealt with in this section. Section 4 elaborates the various issues in the polishing of dielectrics such as silicon di oxide, various doped and undoped oxides and different low-k materials. The section also briefly deals with modeling aspect of dielectric CMP. The polishing of Cu is described in Section 5. The post-CMP clean process of wafers after dielectric and metal polishing step has been discussed in Section 6. Novel post-CMP clean process and materials used for these processes have been discussed in the section. The final section concludes with the gist of the paper and gives an idea of the future trends that the CMP process development is expected to follow.

2. Chemical mechanical polishing process

2.1. Evolution of chemical mechanical polishing

By definition, chemical mechanical polishing is a process whereby a chemical reaction increases the mechanical removal rate of a material. CMP is mostly used for material removal by polishing the ''hills'' on the wafer and ''flattening'' the thin film. The chemical reaction between the slurry and wafer is tailored to enhance material removal and bring about quicker planarization of the thin film.

2.1.1. History

The modern day application of CMP process in the semiconductor industry was for polishing the surface raw silicon wafers to achieve a global flatness over raw silicon wafers. After sawing, the single crystal silicon rod and removing the mechanically damaged surfaces, the wafer needs to be flattened globally and a uniform scratch free surface needs to be made available for fabrication of semiconductor devices. The idea of using colloidal silica, then made by Monsanto, instead of standard abrasives, was developed by Bob Walsh in 1961 [59] and thus, the first wafers polished using CMP were commercially available in the early 1960s [59,60]. Before its implementation in polishing raw single crystal silicon wafers, the process of CMP was traditionally used in glass polishing. One of the most wide spread application of CMP outside the semiconductor industry is optical lens polishing. In fact, the first machinery used by Monsanto was very similar to the commercial machine used in the optical industry. The first semiconductor CMP machine was an innovation of the optical lens polishing machine. The proper polishing abrasives in presence of the slurry chemicals were used to achieve a superior degree of precision and flatness to meet the demands of the semiconductor industry. By supplementing mechanical polishing with high hardness abrasives such as silica in an alkaline medium, there are significant gains in material removal and reduction the process time.

A further improvement to the CMP process was made at IBM in the late seventies and early 80 s. The new process was faster than the previous silica-based polishing method and resulted in ultra flat, ultra smooth surface to meet the stringent requirements of the IC industry [61]. The slurry was later tailored to reduce defects and surface non-planarity introduced by the etching and deposition processes.

The IBM process was then applied for trench isolation by the late 1980s in Japan for various logic and DRAM devices. There was wide spread industrial implementation of the different variants of the CMP by companies such as NEC, National Semiconductor, Hitachi, etc. This led to the introduction of the first commercial polisher designed specifically for CMP by Cybeg in Japan in 1988. Later, International SEMATECH identified CMP as a technology critical for the future of IC manufacturing and launched a project to develop competitive, advanced CMP tools in the US [62].

2.1.2. CMP process in the future

The semiconductor industry has effectively adapted its CMP technology for the 300 mm wafer [63]. Beyond the adoption of copper interconnects, several technologies are necessary to continue the shrinkage of device dimension and the increase of packing density in ULSI manufacturing. The use of ultra low-k materials as interlayer dielectrics has been at the forefront for decreasing the ''C'' of the ''RC delay''. However, polishing of ultra low-k dielectrics which are soft mechanically and weak is a daunting task in itself. The single and dual damascene structures comprising of ultra low-k porous or polymeric materials are more prone to buckling and crushing failures. It can be seen from Fig. 24, that these materials have significantly lower hardness and Young's modulus as compared to silicon di oxide which has a dielectric constant of about 3.2–4.0 available in the market today. According to the ITRS

roadmap [14] materials with dielectric constant 2.2 will be integrated in the IC by year 2007 (Table 5). The difference between the polishing rates of copper and the low-*k* materials available will significantly affect post-CMP surface planarity. New processes must be developed to address the problems associated with this non-uniform polishing phenomenon as well as the complexity of the materials structures. Also, there needs to be a marked improvement in slurry selectivity for accurate

Table 5
Tabulation of interconnect international technology roadmap for semiconductors [14]

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU/ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Number of metal levels	8	8	8	9	10	10	10
Number of optional levels—ground planes/capacitors	2	2	4	4	4	4	4
Total interconnect length (m/cm^2)—active wiring only, excluding global levels [1]	4086	4843	5788	6879	9068	10022	11169
FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	1.22	1.03	0.86	0.73	0.55	0.50	0.45
Jmax (A/cm^2)—wire (at 105°C)	9.6E5	1.1E6	1.3E6	1.5E6	1.7E6	1.9E6	2.1E6
Imax (mA)—via (at 105°C)	0.32	0.29	0.27	0.24	0.22	0.20	0.18
Local wiring pitch (nm)	350	295	245	210	185	170	150
Local wiring A/R (for Cu)	1.6	1.6	1.6	1.7	1.7	1.7	1.7
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	28	24	20	18	16	14	13
Intermediate wiring pitch (nm)	450	380	320	265	240	215	195
Intermediate wiring dual Damascene A/R (Cu wire/via)	1.6/1.4	1.6/1.4	1.7/1.5	1.7/1.5	1.7/1.5	1.7/1.6	1.8/1.6
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	36	30	27	23	20	18	18
Minimum global wiring pitch (nm)	670	565	475	460	360	320	290
Global wiring dual Damascene A/R (Cu wire/via)	2.0/1.8	2.0/1.8	2.1/1.9	2.1/1.9	2.2/2.0	2.2/2.0	2.2/2.0
Cu thinning global wiring due to dishing and erosion (nm), 10% × height, 80% areal density, 15 μm wide wire	67	57	50	48	40	35	32
Cu thinning global wiring due to dishing (nm), 100 μm wide feature	40	34	30	29	24	21	19
Conductor effective resistivity (μΩ-cm) Cu intermediate wiring	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	16	14	12	10	9	8	7
Interlevel metal insulator —effective dielectric constant (κ)	3.0-3.6	3.0–3.6	3.0–3.6	2.6–3.1	2.6–3.1	2.6–3.1	2.3–2.7
Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ)	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4	<2.1

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

end point detection when the constituent layers of the damascene structure namely, metal, hard mask, cap layer, barrier layer and dielectric are polished [64]. Further more, it is necessary to explore the niche of the CMP process in shallow trench isolation and other applications such as backside polishing and the fabrication of micro-electro-mechanical systems (MEMS). The CMP process there must be integrated horizontally and vertically to achieve high thorough put and performance. In MEMS applications horizontal integration ensures reliability and good performance of a specific CMP process run. The development of new polishing pads and pad architecture, novel slurries, new metrology techniques, etc. comes with in the scope of horizontal CMP integration. Vertical integration ensures success of every successive CMP operation. This includes the integration of the upstream processes such as Cu/barrier deposition and etching and downstream processes such as ILD deposition and lithography. This opens a wide scope for research for further optimization and development of Cu CMP process.

2.2. CMP a multistage process

The recent developments in the semiconductor industry described previously imply that CMP is fast becoming the established technology for planarizing metal and interlayer dielectrics of multilevel sub-0.5 μm devices. Along with the rapid growth of CMP and its application for polishing various materials, have come a variety of slurries, different pads, complex process recipes, more complex slurry mixing and distribution systems and an increase in the volume of wastewater. Polishing of different materials and customized needs of the various semiconductor industries have given birth of more complex CMP equipment with different process dynamics such as linear, orbital and fixed head machines. Reliable filtration and waste distribution are also required to avoid hazardous environmental implications, as the increase in the number of CMP process steps have given rise to a large amount of disposable slurry waste. The schematic of the industrial CMP process (isolated from the other process in the fabrication line) is as shown in Fig. 16.

As seen from Fig. 16, the slurry is mixed in a tow at a central location from where it is distributed to the various CMP machines in the fabrication. The slurry that not used for feeding any machines is then returned back to the tow for recirculation. The slurry that is used for CMP process is later disposed

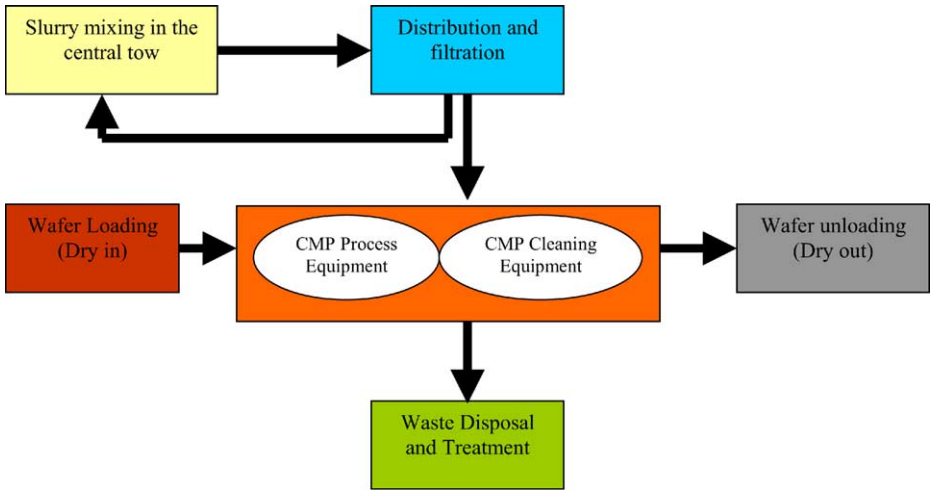

Fig. 16. Schematic of the industrial CMP process isolated from the other process.

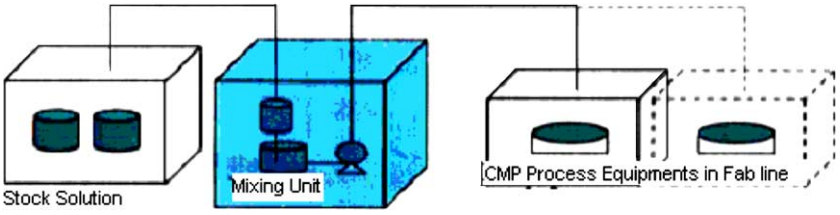

Fig. 17. Schematic of the slurry mixing at a centralized location.

off. The wafer which is dry from the previous process is loaded in the CMP process equipment where it undergoes polishing and then cleaning. It is then dried in the CMP cleaning station (which may be integrated with the polisher). Most machines follow this dry in dry out methodology.

2.2.1. Slurry mixing

CMP slurry feeder equipment is composed of a stock solution unit, a mixing and circulation unit, and the CMP equipment. The thick slurry supplied from the stock solution unit is diluted to a fixed density in the mixing and circulation unit using ultra pure water. The mixed and diluted solution is then supplied to the CMP equipment. All of the equipments are manufactured in a clean room with high degree of cleanness, under strict quality checking. Consistent construction method is used from the manufacturing of the slurry feeder unit to local piping, wiring, cleaning and the trial run adjustment of the system. The system thus needs to be of high quality and stability. A tolerance of about 1% is maintained in meeting the recommended slurry parameters. The schematic of the slurry mixing is shown in Fig. 17.

In this section, the various physical aspects of the CMP process are discussed in detail in order to give a better understanding of the general working of the industrial CMP process and the various parameters associated with it [65].

2.2.2. Slurry distribution system

Fig. 18 gives a simplified physical representation of a semiconductor fabrication line in which, the slurry distribution to the various CMP tools is shown. As seen from the diagram, the slurry is mixed and blended at a centralized location from which it is distributed to the various machines through the distribution lines. The distribution loop shown in the schematic ensures that the ‘‘good’’ slurry, which is unused for the process, is delivered back the mixing chamber or the tow, in order to prevent slurry

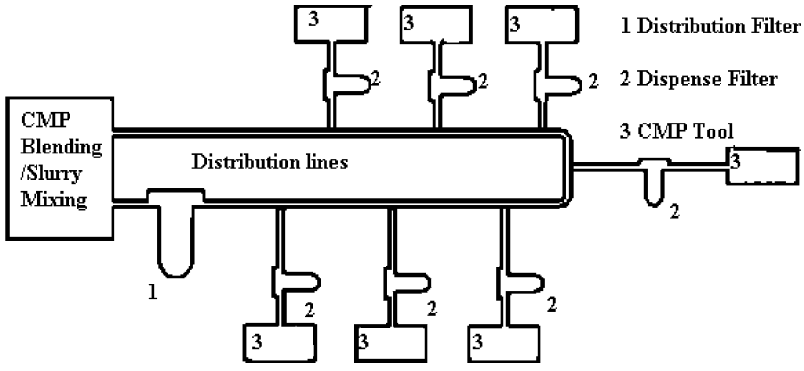

Fig. 18. A schematic of CMP slurry distribution system [68].

wastage. Although CMP slurries are composed of very fine particles up to 200 nm (0.2 μm), ''large'' particles of 1–3 μm and greater are often present in slurries at the point of dispense. Such particles can be formed as a result of agglomeration or the presence of foreign material. Metal CMP slurries, in particular, are prone to formation of aggregates. The agglomerated slurry particles often cause numerous defects in the wafer during CMP. Microscratching is the most prominent defect which occurs mainly due the agglomerated particles present in the slurry delivered to the machine as well as such particles embedded in the pads [67]. This makes the continuous mixing of the slurry in the tow absolutely imperative. In order to prevent the particle agglomeration [67] during the distribution stage, dispense filters are installed on each of the machine which filter out the agglomerated particles before slurry delivery. Care must be taken that the filtration of the agglomerated particles does not change the particles distribution and concentration of the slurry. Most often, a series of filters are used in order to minimize the drop in the slurry pressure and flow. The slurry after being used for the actual CMP process in the tool is then disposed off using appropriate methods and environmental damage is restricted [68].

2.2.3. CMP process

Current semiconductor fabrication technology for logic and memory devices requires CMP to achieve the required multilevel interconnections densities. Indeed, each silicon wafer can be exposed to 15 or more CMP steps before final device assembly. A schematic diagram of the CMP process is shown in Fig. 19. During CMP, the wafer is pressed face down against a rotating polishing pad, while a chemically and physically (abrasive) active slurry planarizes the wafer. As wafer size grows, devices sizes shrink and process requirements grow more stringent, within die/wafer uniformity and removal rate increase becomes a greater concern. Different CMP processes attempt to achieve a balance between removal rate and global/local planarization through a combination of solution chemistry, speed, applied pressure and pad properties [56,65]. Often a change in slurry or operating conditions lead to conflicting performance.

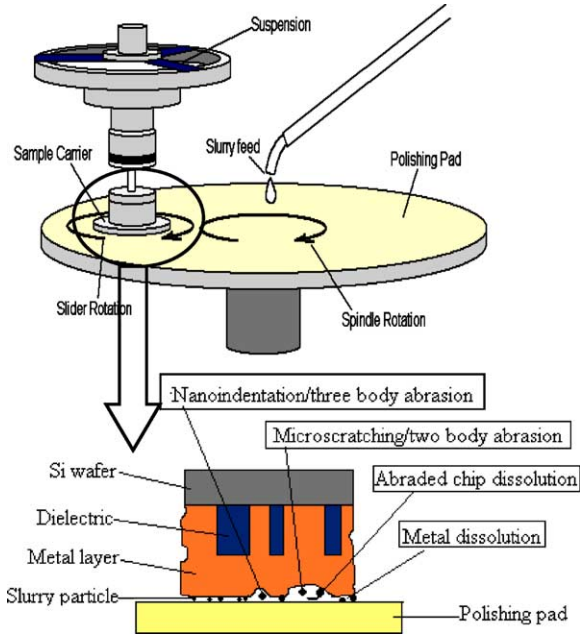

Fig. 19. Schematic diagram of the CMP polishing process.

2.2.4. CMP polisher considerations

The key issues affecting industry use of CMP during the semiconductor chip manufacturing are the high cost of ownership (CoO), the lack of industry wide CMP technology and less than thorough understanding of the knowledge of the underlying science behind the CMP process [65]. Improvement in CoO has been brought about in the fast few years due to: (1) higher raw throughput; (2) in situ film thickness metrology; (3) dry in dry out configuration ensuring low defectivity [68]; and (4) process equipment, implementation and integration support from CMP vendors [68].

The first generation CMP tools based on rotational platen had low throughput values of about 10–18 wafers/h [65]. The second generation tools emphasized on evolutionary improvements while the third generation equipment designs were modified to stay in production for long period of time by giving them adaptability to future technology modifications. The throughput of the machine can be enhanced by increasing the removal rate and improving the wafer handling. However, for effective CMP of materials, the increase in removal rate by increasing the down force should not be brought about by compromising on the defectivity (like increase in wafer to wafer and within wafer non-uniformity, delamination, dishing, erosion, etc.) [70,71] of the wafer. For this reason sometimes, the throughput is compromised to polish the wafers at lower down force there by increasing the polishing time. The efficiency of the robot handling of CMP machine also determines the throughput of the machine [72].

2.2.5. First generation CMP polishers

The first generation CMP polishers use a single robot system to move the wafer and hold it on the carrier. The polisher is comprised of two rotating platens; one covered with a hard pad for bulk material removal and other with relatively soft pad for buffing. The wafer is pressed face down on the pad by the carrier and the slurry is deposited close to the center of the pad, from where the centrifugal force spreads it all over. The mechanical properties, surface morphology, structure, absorbency, etc. strongly affect the slurry distribution and polishing [73]. The polishing platen on these tools is around 22 in. in diameter which is more than 7.5 times the size of a 200 nm wafer [65]. The actual slurry utilization of these processors is poor and the pH of the slurry changes during use as there is an absence of any slurry reprocessing unit [74]. The amount of slurry that is actually used for processing at the interface is function of pad properties [75], pad conditioner [76], pad topography [77] and slurry viscosity [78]. Thus, the pads must be conditioned to (1) bring the pad back to flat; (2) remove materials from pores; and (3) rebuild the nap. Simple manipulation of the machine parameters is sufficient to increase the material removal rate in these polishers. However, issues such as platen wobble need to be taken care off in order to deliver CMP wafers in the acceptable range. The schematic of the first generation polishers is similar to that shown in Fig. 19.

2.2.6. Second generation CMP polishers

The second generation polishers like, are basically made of rotating carrier and platen designs but have numerous changes to improve the raw throughput. The second generation polishers can be classified broadly in two distinct types: (1) single large (22 in.) platen polishing numerous wafer concurrently on the same pad, and (2) single wafer per platen, multi-platen systems. The improved thorough put range has been quoted to be around 30–60 wafers/h [65].

2.2.6.1. Multi-wafer per platen polishers. There is a natural increase in the throughput due to the increase in the number of polishing heads per platen. However, this approach presents several challenges. The most severe issue is the quantity of the wafer put at risk at one time. If one wafer breaks, the pieces can damage several wafers at one time. The more subtle issue is that of load balancing. As long as all the carriers on the platen are loaded with wafers, polishing can be consistent.

Fig. 20. Schematic of multi wafer per platen polisher [78].

However in certain cases, like application specific integrated circuit (ASIC) fabrication where in just one or two wafers need to be polished at one time, this issue is of considerable importance. The schematic of multi wafer per platen polisher is shown in Fig. 20.

2.2.6.2. Sequential rotational systems. Another approach usually adopted to avoid the risk of damaging more number of wafers due to pad anomalies is sequential polishing of wafers on different platens. This approach involves multi-step polishing wherein the first platen is used for bulk material removal without particular regard to superficial surface defects, the second platen is used for global planarization while the third platen is used to for a fine buff to get a defect free mirror like surface. However, synchronization of all these processes is an issue that the process engineer needs to tackle with this approach. This implies the process speed is limited by the slowest process. This is especially a problem when polishing metals such as copper as the corrosion might results due to the wafer staying wet in the slurry for a longer duration of time [79,80]. Also, small damage to the pad can result in damage to all wafers in the sequential polishing run and it is sometimes hard to determine the damage on the pad and hence, all pads need to be changed. In case of tool failure, all the processes need to be

Fig. 21. Sequential rotational CMP polisher [69].

stopped until repairs and tool utilization is limited due to tool inflexibility. Fig. 21 shows an illustration of sequential rotational CMP polisher.

2.2.7. Third generation polishers

The third generation polishers have a series of evolutionary and revolutionary systems built in them or integrated in them as modules. Dry in dry out feature is one of the most prominent enhancements in this kind of polishers. This considerably reduces the wafer defects especially in metal CMP as corrosion of the metal is drastically reduced as a result of cleaning after the polishing step. The addition of in situ metrology modules such as motor current detection [81], sensor array for integrated steering [82], thin film reflectivity [83] in situ optical end point detection method [84] have markedly improved CMP process performance and reduced defectivity. There are several new end point detection and other metrology modules such are integration of acoustic emission sensor [85], force sensor [86] and Cu radioactivity detection [87] that are candidates for implementation in the third generation polishers.

2.2.7.1. Sequential linear polishers. The sequential linear third generation polishers are generally used in CMP for STI and rarely in ILD structures. The polishers have a moving belt on which the wafer is pressed device side down and rotated slowly about the carrier axis. The belt which is held in tension between rollers moves rapidly [88]. This type of polisher can achieve high removal rate owing to high belt speed and can achieve faster planarization as for STI application where large amount of material needs to be removed from a relatively lower pattern density structure. The low down force and high relative velocity polishing regime limits the damage to the film [13]. The linear polishers require new set and architecture of polishing pads which comprise of single polyurethane belt without foam or felt (sub-pad). The concurrent polishing pad conditioning is obtained by means of a novel polishing pad design where polishing pads have to be mounted in a cylindrical configuration and not on a the conventional flat surface configuration [89]. A special polishing pad conditioner is provided to refurbish the polishing pad [90]. With more and more publication of data showing improved CMP performance at low down force and high linear velocity, this type of polisher is finding increasing acceptance in the semiconductor processing industry. Fig. 22 shows a photograph of a sequential linear polisher.

2.2.7.2. Orbital polishers. Several CMP tool concepts have been developed based on orbital motion. Some orbit the carrier with rotating the carrier [91–93] while others orbit the platen while rotating the

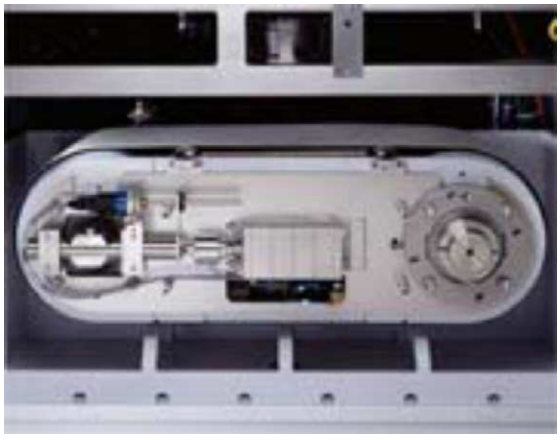

Fig. 22. Illustration of the polishing action during linear polishing action [97].

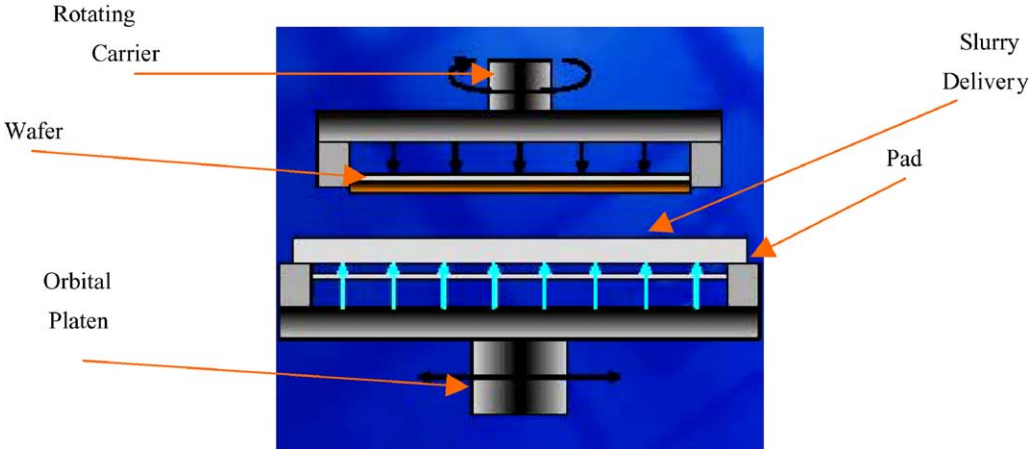

Fig. 23. Schematic of rotary CMP polisher [13].

carrier [94]. Some of the polishers also involve arbitrary non rotational motion on a fixed polishing pad. In these types of polishers the fundamental principle of relative motion between the wafer and pad to remove the material is used, however, unlike the first generation polishers, slurry is delivered directly at the pad area used for polishing thus improving slurry utilization efficiency. The schematic of the orbital polisher is shown in Fig. 23. The preferred mode of operation of orbital polishers is low down force with high relative velocity. With the recent popularity of the contact retaining ring method for polishing, the pad remains compressed at the edges of the wafer and reduces the area of the die lost due to edge exclusion [95]. The planarization capabilities of these tools are known to be better than the first and second generation polishers. These of machines are also known for their small down times due to the rapid change individual polishing heads.

2.2.7.3. Rotary inverted. In recent years, Nikon Inc. has developed high-precision CMP systems applying proprietary technology based on its long experience in lens polishing and optical measurement [96]. The system's special face-up polishing uses small pads applied at very low pressure and high-speed rotation. The compact polishing pad as seen in (Fig. 24a) enables high-speed rotation. Its light-weight, less pad deformation feature allows superior planarity. These features are especially advantageous ultra low-k polishing process. Through the compact polishing pad the slurry is supplied onto polishing area of the wafer efficiently. This enables less slurry consumption compared to the conventional polishing equipment (Fig. 24b). Face-up polishing at the polishing station enables continuous optical end-point

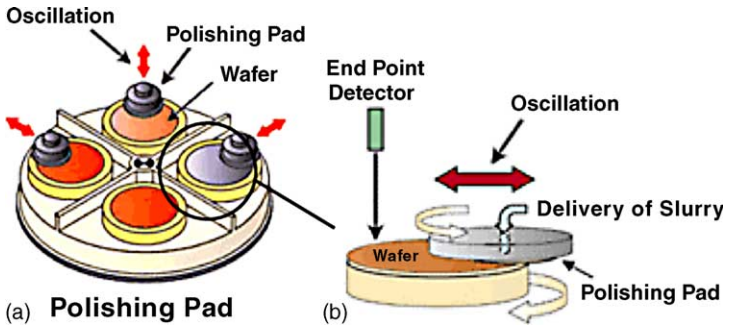

Fig. 24. (a) Set up of multi wafer rotary inverted CMP polisher and (b) polishing action and end point detection [96].

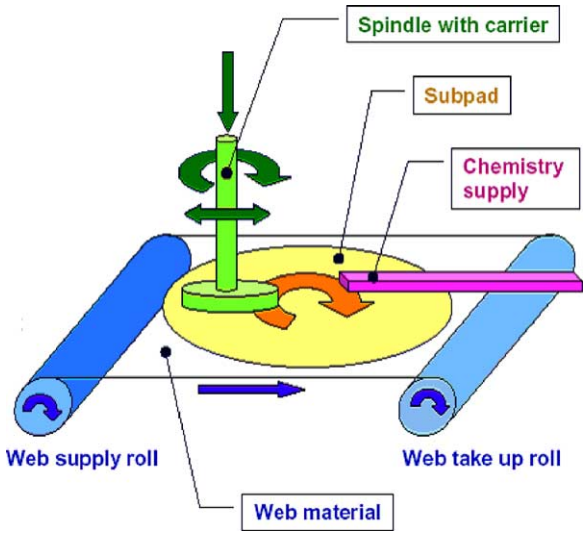

Fig. 25. Schematic of a web-type polisher [98,99].

measurement. It helps improve S/N ratio while minimizing slurry effect for end-point detection. Mounting of wafer and pad are also convenient with this system. In spite of some initial excitement about this system, it is yet to have a proven track record in the semiconductor fabrication environment.

2.2.7.4. Pad feed polishers. The pad feed polishers are based on a recently developed pad type that is held in rolls. These polishing pads are fed to the wafer polishing tables, the wafer is polished, pad is conditioned and then the pad moves further (Fig. 25). This methodology is especially useful for pads that have very repeatable first polish performance and their characteristics either degrade or change with subsequent polishing runs. This polisher unlike others does not have to be turned off for changing the pad there by maximizing the equipment utilization time [97,98]. This technology is still in its nascent stage and various industrial giants continue to develop it even further in order to make a positive impact on the CMP polisher market. The details about the fixed abrasive pad that is mostly used in this type of polishers will be discussed in the consumables section of the paper.

2.3. CMP interactions

The wafer–pad interfacial chemical reactions in the presence of the slurry for oxide and copper have been discussed briefly before and will be discussed in detail in the respective sections. These reactions are characteristic to the respective materials of this three-body abrasion system. The force field analysis on the pad and wafer during the CMP process and summation of the input and output variables that affect the CMP process have been discussed in this subsection. The contact mechanics and mechanics of material removal, fluid dynamics of the slurry, effect of heat transfer, modeling and simulations of the various parameters affecting the CMP output will be discussed in the modeling section.

2.3.1. Force field analysis

In 1927, the Preston equation was developed (Eq. (2.1)) [99], which models the mechanical effects of pressure and velocity in the CMP process:

$$R = KPV \tag{2.1}$$

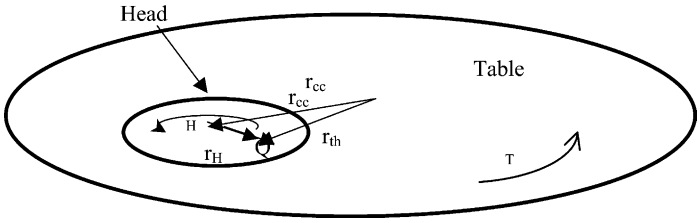

Fig. 26. Schematic of the force field on the wafer and the pad during CMP [37,70].

where R denotes the polish rate, P is the applied downward pressure, V is the linear velocity of the wafer relative to the polishing pad, and K is a proportionality constant, called the Preston coefficient.

As seen in Fig. 26, r_{cc} is the linear distance between the centers of the wafer carrier and the platen, which is mostly assumed to be constant, r_H (H stands for head) is the positional vector at any point Q on the wafer from the center of the carrier and this varies with the position of the point Q, r_{th} is the positional vector of any point Q on the wafer from the center of the platen (this distance varies with the location of Q). V_Q is the velocity of any point Q on the wafer. V_T and V_H are the linear velocities of the table (platen) and wafer head. ω_T, ω_H are the rotational velocities of the platen and wafer carrier. Assuming that $\omega_T \neq \omega_H$ velocity V_Q will vary from point to point over the wafer. The variation in velocity will call cause changes in the removal rate across the wafer in accordance with the Preston's equation.

$$r_{th} = r_{cc} + r_H \tag{2.2}$$

$$V_Q = V_T + V_H = -(\omega_T \times r_T) + (\omega_H + r_H), \quad \text{where } V_Q = (\omega_T \times r_{cc}) = [r_H(\omega_T - \omega_H)] \tag{2.3}$$

However, if ω_T is set equal to ω then linear velocity will be independent of the location of the wafer for $V_Q = -[\omega_T \times r_{cc}]$. This with the V_Q maintained as shown before, the velocity of all points on the wafer will be the same and then there will be no change in the removal rate of the material. This force field analysis is taken in to account to fundamentally design any CMP process [37,70]. In any event, many times, the process engineers are still confronted with the problem of wafer to wafer and within wafer non-uniformity (WIWNU and WTWNU) (Fig. 27) [33].

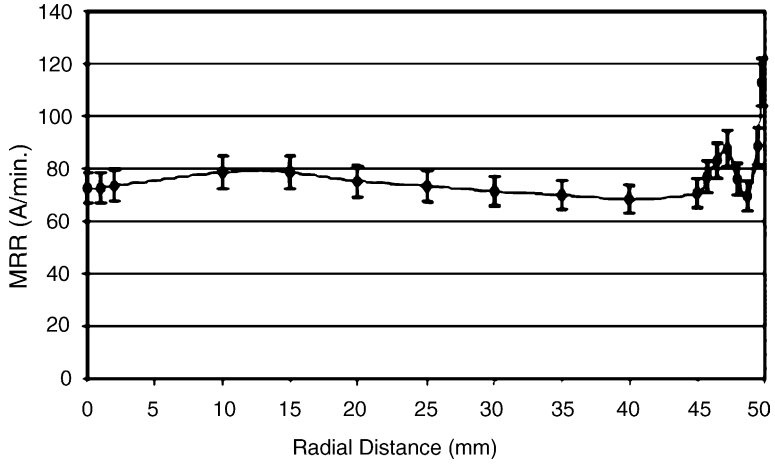

Fig. 27. Non-uniformity in removal rate with in a wafer [33].

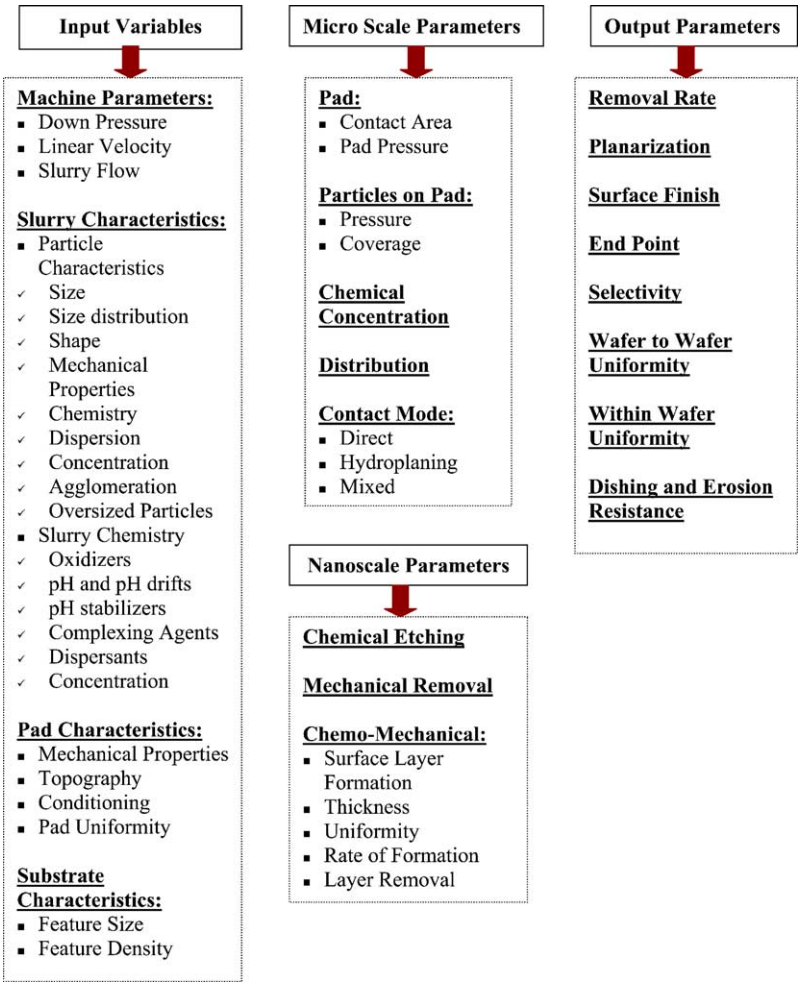

Fig. 28. Parameters governing the CMP dynamics [101].

2.4. *Parameters governing CMP*

Parameters and variables that govern the CMP process have been illustrated in Fig. 28.

2.5. *Influence of machine parameters*

The CMP process combines mechanical and chemical removal mechanisms in a synergistic effect. This synergy has been the subject of many studies, but focus in the past has been primarily on mechanical effects due to the difficulty of identifying the reaction mechanisms of the chemical effect. However, mechanical effects alone cannot provide the type of polishing necessary for IC manufacturing. Chemical effects contribute to the increased global planarity and reduced micro roughness required for successful IC fabrication. As discussed in the earlier section, the fundamental basis for designing any CMP process module, the force field analysis of the wafer–pad–slurry abrasion system is made. The variations in the machine parameters to obtain optimal results are the first adjustments made to refine the CMP process. Until recently, slurry flow and slurry flow rate was not given much importance variation of machine parameters [65], however, with the ever-growing demands for

enhanced yield and low defects, and also with the knowledge of the heat transfer behavior of the slurry [100], the slurry flow is also brought in the CMP process control equation. This section discusses the broader impact of these machine parameters on the CMP process. A better understanding on the effect of machine parameters on the CMP process can be obtained by performing repetitive CMP experiments on a prototype CMP tester in which process data is monitored in situ. CETR bench top CMP tester has been used by Sikder et al. for studying the CMP process in detail. The details of the CMP tester can be obtained in literature [102]. The polishing tests on the CETR tribometer were performed on (1 in. × 1 in.) PECVD SiO_2 using Klebesol 1501 (Rodel Inc., DE) colloidal silica slurry (pH 10–11) on an IC 1000/IV pad with linear velocity 5 mm/s and a radial distance of 50 ± 2.5 mm. The down force used was 4 psi and the platen rotation was 150 rpm. Influence of machine parameters such as down force, relative velocity, slurry flow on the acoustic emission (AE), coefficient of friction (COF) and removal rate (RR) was observed. For removal rate calculations, thickness of oxide was measured at nine points using the ellipsometer. The wear rate was calculated by re-measuring the sample after polishing at nine points.

2.5.1. *Coefficient of friction*

COF is an important tribological property of films and pad, and was recorded during all the tests. Fig. 29a and b shows the COF versus rpm and psi, respectively, during polishing. With higher rpm, COF decreases, whereas, decrease of COF is very small with the increase of psi. COF has marked effect on removal rate, local and global uniformity. Value of COF has influence in polishing performance, which is discussed in the next section.

2.5.2. *Effect of polishing conditions on removal rate*

Figs. 30 and 31 show the removal rate as a function of rpm and psi, respectively. Experiments on two sets of samples show the same trend. Removal rate increases with both rpm and psi. Removal rate decreases slightly at platen rotation 250 rpm. This may be due to inadequate slurry flow under the sample at higher platen rotation. As COF decreases with increasing rpm and psi, a lower COF may be

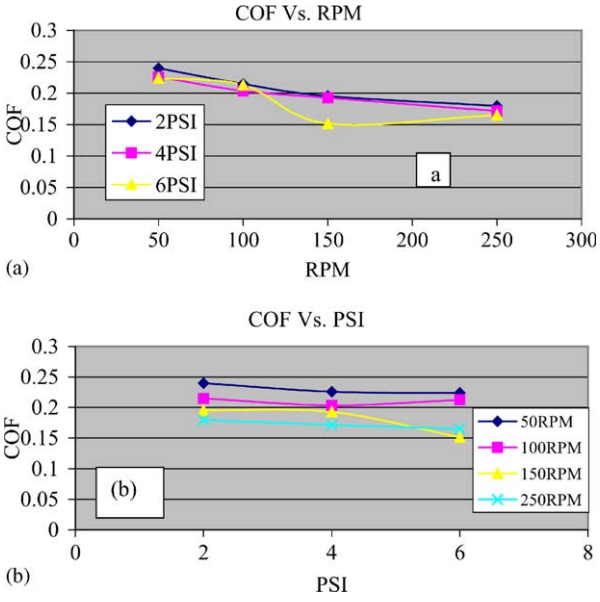

Fig. 29. Average removal rate with rpm at different psi for two sets of samples [102].

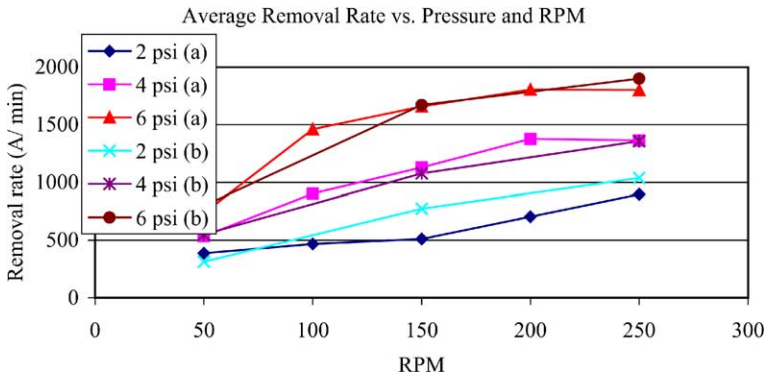

Fig. 30. Average removal rate with rpm at different psi for two sets of samples [102].

related to the higher removal rate in CMP process. Fig. 32 shows the removal rate versus rpm × psi and the linear relation indicates that polishing of oxide follows Preston's equation [99].

2.5.3. *Importance of slurry flow*

It is important to optimize the effect of slurry flow rate on the COF and AE signal. Results of the optimization experiments are summarized in Table 6. It can be seen from Table 6 that COF decreases slightly while no significant change can be noticed in AE signal. Decrease of COF may be attributed to the higher slurry flow rate during polishing. Therefore, the data suggests that flow rate may not affect the AE signal.

The flow pattern of the slurry on the pad affects the polishing rate as well as the WIWNU. Due to the rotation of the lower platen the flow pattern will be different as we feed the slurry at different positions of the pad. Fig. 33 shows the different positions of slurry feeding on the platen. If the slurry cannot reach uniformly at the pad-film contact points material will not be removed uniformly. It can be seen from Fig. 34 that center position and position "8" (very near to the center) are two better positions to feed slurry while platen is moving clockwise.

The friction generated during CMP brings about over all increase in the temperature at the wafer pad interface. Certain CMP processes such are silicon polishing are exothermic. Hence, there is a natural increase in the temperature at the interface. The increase in temperature changes the reaction kinetics of the slurry with the wafer, mostly increasing the removal rate. However, the increase in

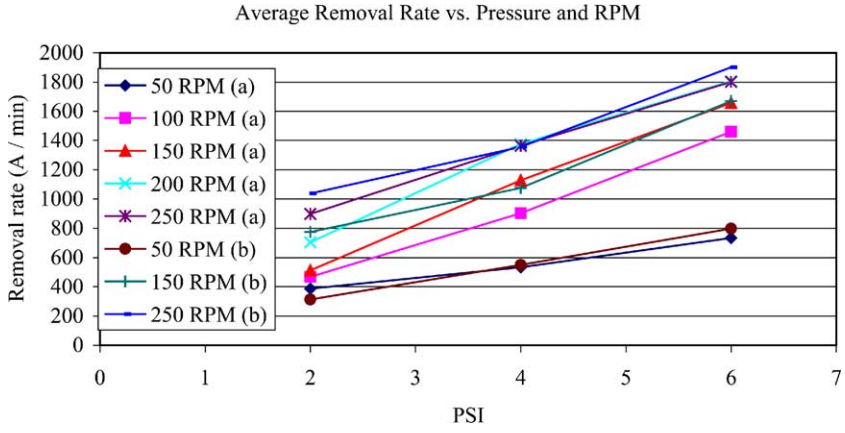

Fig. 31. Average removal rates with psi at different rpm for two sets of samples [102].

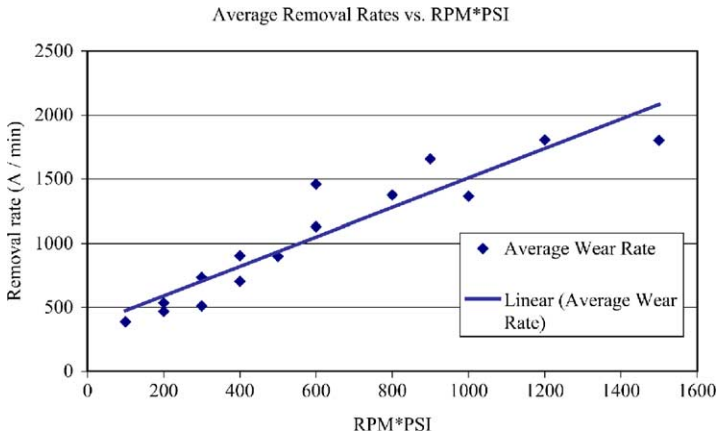

Fig. 32. Average removal rates plotted with rpm × psi. Linear relation indicates that polishing follows Preston's equation [103].

Table 6
Effect of slurry flow rate on the COF and AE signal for experiments performed [102]

Run #	Slurry flow (ml/min)	COF	AE signal (arbitrary unit)
1	35	0.3977	0.4013
2	75	0.3949	0.4533
3	100	0.3932	0.4184
4	155	0.3911	0.4133
5	195	0.3888	0.4189

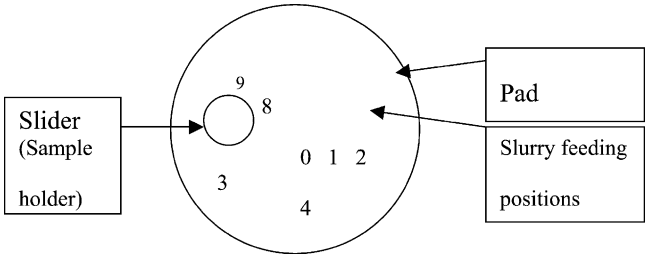

Fig. 33. Schematic of the positions of slurry feeding on the pad during polishing for feeding position optimization. Distance 0–1.4 = 15 mm, 0–2.5 = 30 mm, 0–3.6 = 45 mm, 0–7.9 = 45 mm and 0–8 = 25 mm [103].

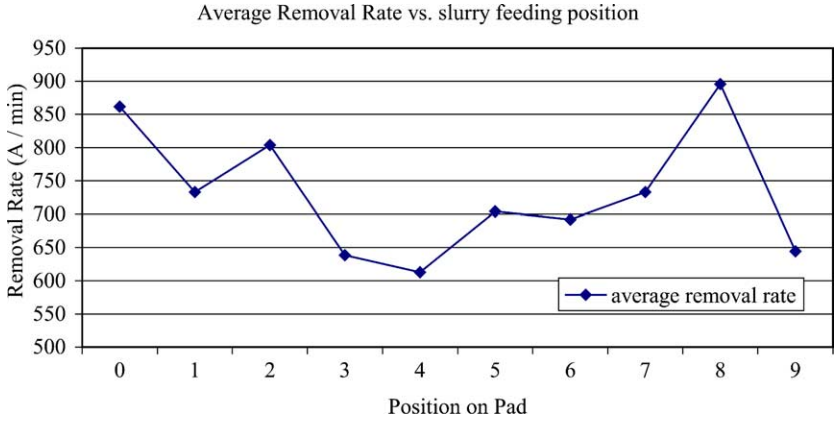

Fig. 34. Average removal rate with the slurry feeding position on the lower platen position [103].

removal rate due to the increased chemical action of the slurry at elevated temperature does not always translate in to greater removal rate during the CMP process [65]. The increase in temperature makes the viscoeleastic polyurethane pad softer, there by reducing the removal rate due to the reduction in hardness [103]. Hence, an optimum slurry flow must be maintained during the process and should be changed if necessary in order to strike a balance with optimum temperature for enhanced slurry action and non-degradation of the pad [65]. Novel CMP process developers have adopted a new recipe to change the slurry flow during the CMP process for optimization of slurry utility and maintaining the temperature during the CMP process [104,105].

3. Chemical mechanical polishing process consumables

3.1. Introduction

The process of CMP has gone thorough as lot of evolution from first being used just for silicon dioxide planarization to the present day planarization applications in pre-metal dielectric (PMD), ILD, STI, metal and gate oxide, etc. The CMP consumables market takes a huge chunk of the present billion dollar CMP market [106]. The research in CMP consumables (pads, slurry, retaining rings) is growing by leaps and bounds [107]. Polishing in its simplest sense is controlled chemo-mechanical material removal to produce a globally flat, defect free surface. This is generally done by rubbing the thin film to be polished with generally a polymeric material, a polishing pad, in presence of the water-based solution containing very fine suspended abrasive particles that are mostly inorganic. Slurry consists of two major components, abrasives and solution. Depending on the material of the abrasives, the chemistry of the slurry, and the synergy between them, each kind of slurry behaves differently [65]. The wafer is held in the carrier and is encircled by a retaining ring which presses the polishing pad down in contact retaining ring type set up [108].

3.2. CMP slurry

CMP is a process that is influenced to a great extent by numerous slurry parameters such as pH, solution chemistry, charge type, concentration and size of abrasives, complexing agents, oxidizers, buffering agents, surfactants, corrosion inhibitors, etc. [56,106,109,110]. The specific and proprietary nature of the slurry manufacture makes it difficult to elucidate the exact effects of slurry on the particular thin films that are polished in it. The slurry interactions at the pad wafer interface are probably therefore, the least understood mechanisms in entire semiconductor fabrication process technology [101]. An ideal CMP slurry should be able to achieve high removal rate, excellent global planarization, should prevent corrosion (in case of metal, especially Cu), good surface finish, low defectivity and high selectivity. The typical design criteria for slurry are given in Fig. 35. These criteria have been broadly identified after survey of literature [111–117].

3.2.1. Global planarization

As discussed in the previous section, the global planarization as a result of CMP process is one of the key outputs of the process. As suggested in Fig. 35 the slurry, plays a key role in achieving global planarization. To achieve the requisite level of global planarization without compromising on the removal rate and producing a defect free wafer surface needs optimization of the slurry parameters. The parameters must be so optimized that the mechanical removal of the material is minimized as slurry depending upon excessive mechanical removal produces high frictional forces and can thus

Global Planarization
- Formation of a thin passivated surface layer
- Minimization of chemical etching
- Minimization of mechanical polishing

Removal (Polishing) Rate
- Rapid formation of a thin surface layer
- Control of the mechanical/interfacial properties of the surface layer
- Stress induction by abrasion to remove the surface layer
- Indentation-based wear
- Fracture/delamination-based removal

Surface Defectivity
- Rapid formation of a thin surface layer
- Minimization of mechanical polishing
- Control of particle size and hardness
- Control of particle size distribution

Selectivity
- Top-layer chemomechanical polishing
- Bottom-layer mechanical polishing
- Reduction of mechanical component in slurry

Slurry Handling
- Formation of stable slurries
- Control of interparticle and particle–surface interactions
- Steric-force-based repulsion in ionic systems

Fig. 35. Prime design criteria for slurry [101].

damage the surface topography. To minimize the frictional forces, the removal rate needs to be compromised and thus the process runs for a longer period of time. Also variation in local polishing pressure leads to variable removal rates within the wafer, which seriously compromises global planarization [101]. Excessive chemical etching adversely affects surface planarity and induces defects on the surface such as corrosion [118]. The key to a good polishing step is achievement of synergy between chemical etching and mechanical planarization with minimization of both the phenomena. For this purpose there is a need for the formation of a passivation layer at the interface of the wafer and pad as seen in Fig. 36. The passivation layer has to be thinner that the difference in the height between high and low regions in order to avoid within wafer non-uniformity [101]. In case of Cu polishing, the formation of the passivation layer is accelerated by oxidizers such as H_2O_2, potassium ferricynate, ferric chloride, and ferric iodate and corrosion damage to the surface is prevented by corrosion inhibitors such as benzotriazole (BTA) [119]. For tungsten, there is rapid formation of surface passivation layers due to the use of peroxygen compounds and stabilizing agents [120]. The purpose of passivation layer in case of silica polishing is to soften the surface which is inherently hard. For this purpose maintenance of alkaline pH in most cases is sufficient [121,122]. During Ta polishing, formation of stable Ta_2O_5 helps in uniform removal of material from the surface [123]. To avoid numerous surface defects, the time to achieve the formation of thin passivation layer should be minimized.

3.2.2. Removal rate

The slurry dependence of the removal rate of a particular material that is being polished is due to slurry chemistry, i.e. chemical action of the slurry chemicals of the material, the mechanical abrasion of the particles on the polished materials, interplay of the different complexing agents, oxidizers and

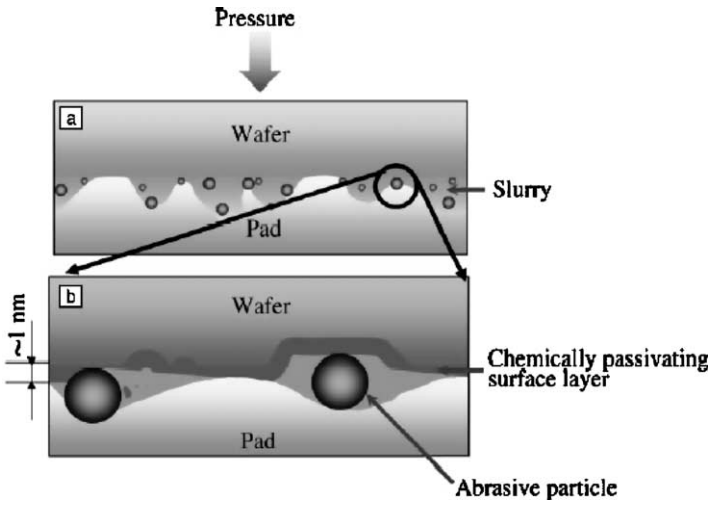

Fig. 36. Schematic diagram of microscale and nanoscale phenomena during CMP [117].

corrosion inhibitors. Chemicals such are oxidizers and corrosion inhibitors vastly affect the reaction rate of the slurry with similar particle nature, size and distributions. Fig. 37 shows the variation of the reaction rate of the different slurry components on Cu when the reaction kinetics were studied using electrochemical chronoamperometry [115,123]. It can be seen from the figure that the surface rate kinetics reaches about 60 Å/s when Cu is immersed in DI H_2O. The reaction rate increases to around 120 Å/s when 5% H_2O_2 is added. However upon addition of 10 mM BTA, the reaction rate came down considerably.

3.2.2.1. Rate of surface reaction. The surface reaction is not the only contributing factor for achievement of high removal rate during CMP. The time scale at which the passivation layer is formed before the average time of successive particle interaction with the wafer for abrasion is also important to produce a defect free, fast CMP process. Fig. 38 shows the electrochemical chronoamperometry (potentiostatic) analysis of Tungsten by first keeping the samples at cathodic potential to avoid surface oxidation and then ''anodizing'' them. The generation of current, which corresponds to surface reaction rate, is monitored on a millisecond scale as shown in Fig. 38. It can be seen form the figure, that Tungsten surface quickly passivates which is conducive for mechanical removal of the material.

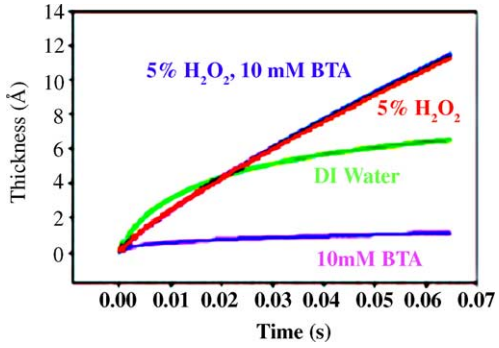

Fig. 37. Variation of rate of surface layer formation in Cu with different slurry chemistry [101].

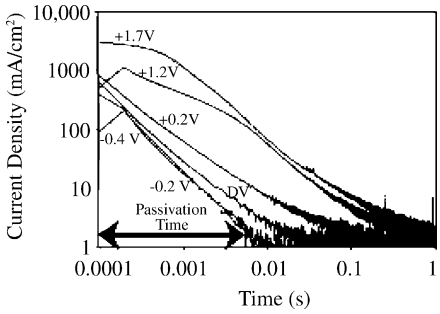

Fig. 38. Transient electrochemical chronoamperometry measurements of tungsten [101].

3.2.2.2. Effect of particle size, hardness and concentration. The generalized materials removal rate (MRR) for oxide has been modeling in the literature and be expressed as shown in Eq. (3.1) [124].

$$\mathrm{MRR} = n\mathrm{Vol}_{\mathrm{removed}} \tag{3.1}$$

The variable n is number of active abrasives taking part in the process and $\mathrm{Vol}_{\mathrm{removed}}$ is the volume of material removed by each abrasive. To estimate the total volume of material removed, it is necessary to estimate the total area of the pad–wafer and wafer-abrasive contact. The area of active abrasive contact is given by:

$$A = \pi x \delta \tag{3.2}$$

where A is the area of contact x is diameter of abrasive and δ is the depth of indentation on the passivating film made by the abrasive particle [125]. If one assumes elastic contact between the particles and the surface, the indentation depth as a function of particle size is given by:

$$\delta = \frac{3}{4}\phi\left(\frac{\mathrm{Papp}}{2KE}\right)^{2/3} \tag{3.3}$$

where ϕ is the particle size, K is the particle fill factor at the surface and E is the Young's modulus of the surface layer [101,125,126]. This equation assumes that the particles are much harder than the surface layer. Eqs. (3.1–3.3) show that the area of contact and indentation depth increase with increase in particle size and hardness. It is thus implied that as particle size and hardness increases the removal rate increases. The increase in particle concentration will increase the number of active particles, there by causing more number of indentations to the passivating film and increasing the removal rate. Fig. 39 indicates the increase in removal rate of tungsten with increase in particle size and concentration. The details of the experiments can be obtained in the relevant literature [101].

Increase in particle size or hardness also gives rise to surface defects such as micro-scratches that cause fatal long-term device failure. Bigger and harder particles would cause deeper micro-scratches, which will be very difficult to eliminate even by the final buffing CMP step. The increase in particle concentration translates in to increase in removal rate only up to a certain extent. As seen in Fig. 40 shown by Singh and Bajaj [101] and Mahajan et al. [113], the removal rate of the silica increases with increase in particle size and concentration at low particle concentration, however after a particular threshold for every given particle size the mechanism of removal changes and there is considerable decrease in removal rate with increase in particle concentration. For the purpose of this experiment, spherical monosized particles were used in slurry of pH 10. Change in material removal mechanism is expected to be the reason of this phenomenon [123].

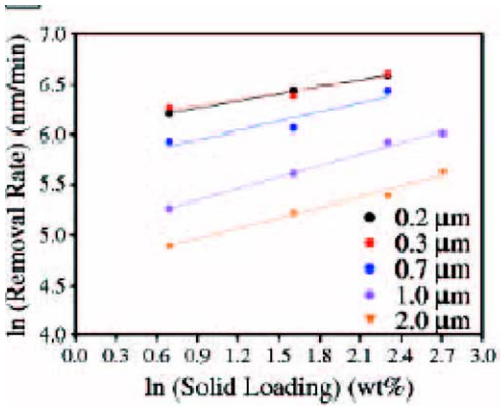

Fig. 39. Variation of removal rate with particle size and concentration [101].

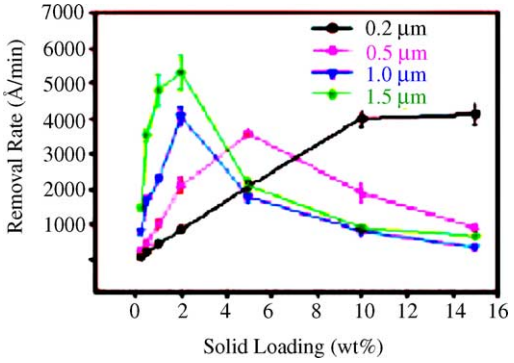

Fig. 40. Removal rate of silica with different particle size and concentration [117].

3.2.2.3. Effect of different particles type. The effect of different colloidal particles in the slurry on the removal rate of the material has been studied by Stein et al. [127]. Potassium Iodate-based slurries (pH 4.0) buffered with potassium hydrogen phthalate (PHP) containing different colloids consisting oxides and hydroxides of cerium and aluminum were used to polish tungsten. The details of the colloids used are given in Table 7.

The variation in the removal with abrasives of similar hardness and size and variation of the process temperature of slurry with similar solution chemistry and different abrasive clearly shows that there is atomistic level interaction between abrasive chemistry and the wafer surface. Thus the surface

Table 7
Details of abrasives used to study tungsten polishing by Stein et al. [127]

Colloid	Metal	Manufacturer	Brand name	Major phases	Size (Å)
3	Cerium	Nyacol	–	Ceriamite	200
4	Aluminum	Nyacol	–	Bohmite (AlO(OH))	500
5	Cerium	Nanophase	Nanotek Ceria	Ceriamite	300
6	Aluminum	Nanophase	Nanotech Alumina	γ-Al_2O_3	300
7	Aluminum	Moyco	Planar W	Gibbsite ($Al(OH)_3$) γ-Al_2O_3 δ-Al_2O_3	–
8	Aluminum	Solution Technology	MET202	Gibbsite θ-Al_2O_3	500

of the colloids can be doctored to produce desirable CMP results such as elevated temperature due to frictional interaction which in turn will improve the process removal rate.

Apart from being influenced by slurry particle size, particle distribution, solution chemistry, additives such as oxidizers and complexing agents, the removal rate is also highly dependent on the material removal mechanism during a particular polishing step. It is common knowledge that removal mechanism of slurry for different materials varies. The details of the removal mechanism of dielectrics and metals have been discussed elaborately in Sections 4 and 5, respectively and are also available in literature [128–135].

3.2.2.4. Particle surface coating. Coating the surface of the particles with harder substance can improve the removal rate while keeping the density of defects constant. The softer particles such as alumina can be coated with a harder surface such as silica to enhance removal rate, while already relative hard silica particles can be coated with cerium oxide particles to improve CMP defectivity [101].

The sub micron abrasive particles for CMP slurry are generally prepared by precipitation techniques based on controlled hydrolysis using method described by Stöber et al. [136]. The methods involving reagents such as ethanol, aqueous ammonia, and water have been widely discussed. The particles fabricated by these methods are dried and redispered in ethanol after ultrasonic treatment for further coating [137]. The harder coating such as cerium dioxide is then coated on the synthesized silica particles by techniques such as precipitation of a cerium salt like cerium nitrate or cerium sulfate in water. The as-precipitated CeO_2/SiO_2 coated powders were centrifuged at high speed, washed with water, dried and calcined. The exact process conditions for coating of silica particles with cerium oxide have been elaborately discussed by Choi et al. [130]. Fig. 41 shows a transmission electron micrograph of silica particle coated with ceria.

To decrease the density of defects in Cu polishing, as well as minimize the dishing erosion damage in SiO_2 and low-k materials, technique of soft abrasion assumes more importance than higher removal rate. For this purpose, special type of slurry abrasive with polymer core and ceramic coating (composite abrasive) has been developed by Yano et al. [138]. Fig. 42 shows the transmission electron micrograph (TEM) of the polymer core, ceramic coated abrasives. The details of the fabrication and separation techniques of these abrasive have been extensively published in literature [139–144].

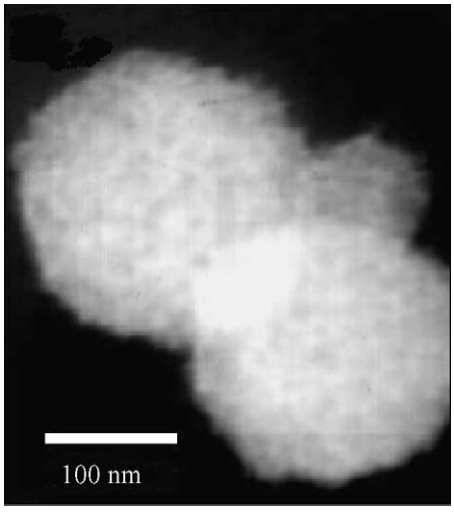

Fig. 41. Transmission electron micrograph of silica particle coated with ceria [1021.

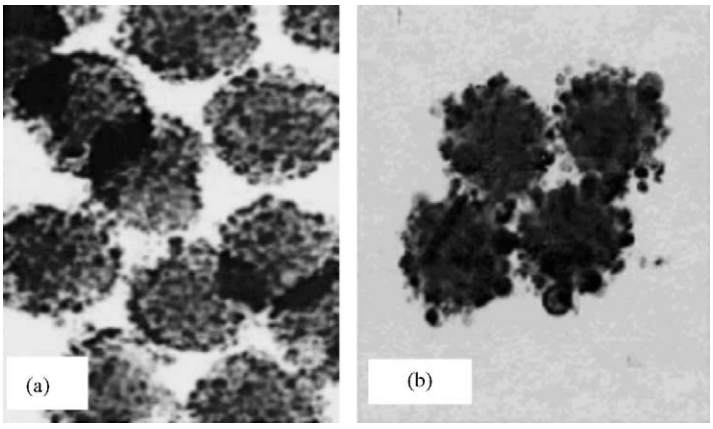

Fig. 42. Transmission electron micrograph of: (a) polymer core SiO_2 coated (diameter 230 nm) and (b) polymer core Al_2O_3 coated (diameter 240 nm) CMP slurry abrasives [140].

Fig. 43 shows the reduction of the dishing and erosion depth when SiO_2 was polished with composite abrasive slurry and conventional abrasive slurry. The total depth of dishing and erosion was reduced to less than 80 nm after first step CMP and less than 70 nm after second step CMP by composite abrasive slurry.

3.2.3. Selectivity

The difference in removal rate of one material as compared to another in a particular slurry gives the measure of the selectivity of that slurry for those two materials. Higher the slurry selectivity, the more effective is the end point detection for a particular CMP process step as there is a marked change in the tribological properties of the material being polished and the under layer. Selectivity is a very important criterion in designing any slurry. For STI, slurry used needs to act on the oxide that is being planarized and not act on the underlying nitride. For polishing Cu, the slurry needs to act selectively on Cu and spare the barrier layer Ta and underlying layers of silica or low-*k* dielectric material. Typically slurry selectivity of 10–25 has been reported for Cu polishing [101]. The selectivity could be considerably improved up to 1000 by introducing particle free slurry [145,146]. The reduction in

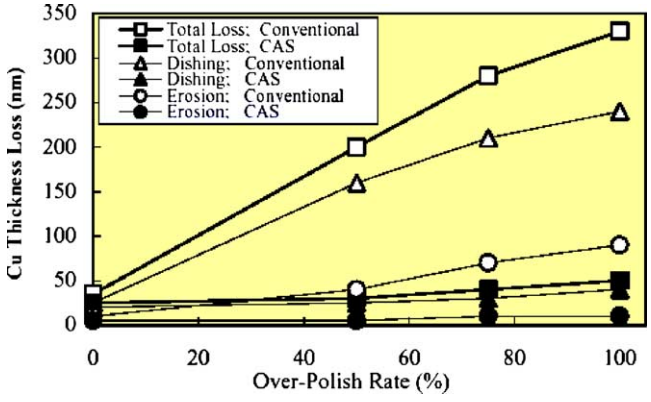

Fig. 43. Comparative dishing, erosion performance of composite abrasive slurry and conventional slurry [142].

mechanical component due to lack of abrasive implies that majority of material removal takes place due to solution chemistry which can be made highly selective.

Slurries with high selectivity facilitate easy end point detection as the tribological properties of the material say Cu being polished in a highly selectivity slurry are markedly different from the properties of the barrier layer Ta or underlying silica layer when polished in the same slurry. The difference in tribological properties can be monitored in situ using techniques such as motor current or force and acoustic emission sensor.

The variation in coefficient of friction and acoustic emission for polishing of blanket Cu, Ta and ultra low-k dielectric (k = 2.2) has been studied. The candidate materials have been polished in the form of 1 in. × 1 in. coupons on the bench top CMP tester (mentioned in Section 2) [102] to evaluate the selectivity of the slurry. The slurries evaluated were: (a) Cu selective alumina particle slurry (Cu1) (a) Cu selective particle less slurry (Cu2); (b) Ta selective slurry with colloidal abrasives (slurry Ta); and (c) non-selective slurry (slurry Cu–Ta). Fig. 44a–d shows the variation of COF and AE at 2 psi and different platen speeds. It can be seen from the figure that the value of COF for a particular material for one polishing condition is unique and hence monitoring the value of COF can give an estimate of the end point of the process. There have been improvements in the effective detection of end point in STI polishing process when high selectivity slurry (HSS) was used and motor current method (which basically used the friction during polishing) was employed.

Addition of specialized chemicals that can act as catalysts in the chemical interaction between slurry and the polished material there by increasing the rate of the chemical reaction with the material being removed considerably is a common approach for improving the selectivity of the slurry. Tetramethyl ammonium hydrate (TMAH) can be added to Cu slurries to considerably decrease silica polishing rate [147,148]. Phosphoric acid added to alumina and colloidal silica TaN slurry has also

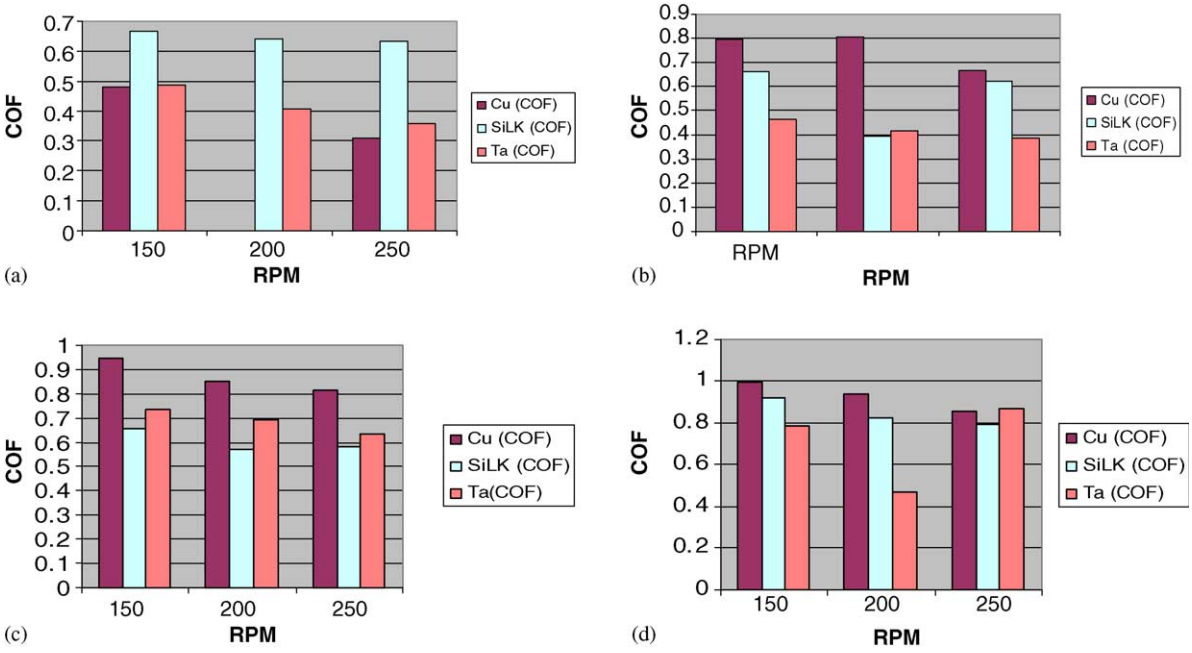

Fig. 44. (a) Variation of COF at 2 psi down force and variable rpm in slurry Cu1; (b) variation of COF at 2 psi down force and variable rpm in slurry Cu2; (c) variation of COF at 2 psi down force and variable rpm in slurry Ta; and (d) variation of COF at 2 psi down force and variable rpm in slurry Cu–Ta [85,86].

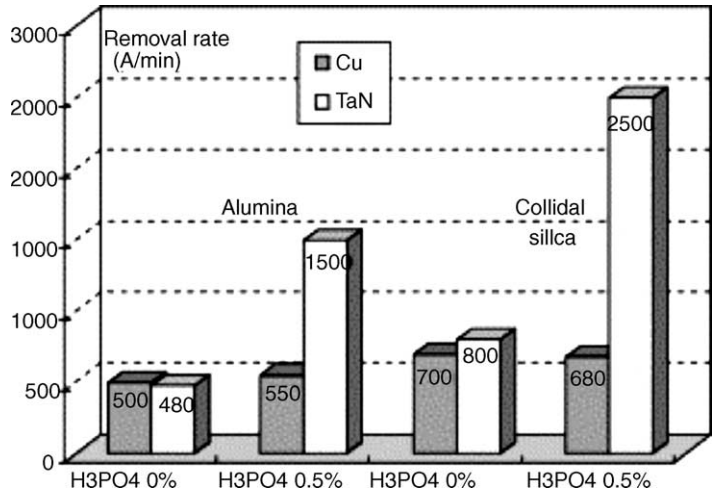

Fig. 45. Cu and TaN polishing result (head 40 rpm, table 40 rpm, and pressure 7 psi) [149].

shown accelerated chemical reaction with TaN. Fig. 45 shows the increase in the polishing rate of TaN with addition of phosphoric acid in alumina and colloidal silica slurry [149].

Mixed abrasive slurries (MAS) containing alumina/silica and alumina/ceria particles have been developed with a goal to improve the selectivity of the CMP slurry [150]. Certain alumina/silica abrasive concentration of MAS has shown marked increase in selectivity for underlying tantalum when Cu was polished while a different concentration of ceria and alumina has shown excellent polishing for oxide over nitride. The details of the experiments with these novel mixed abrasive slurries have been published by Jindal et al. [151].

The reduction of the mechanical components by using smaller colloidal particles or making the particles softer or porous can drastically improve the selectivity. The particle surface modification will be discussed later in the section. Though highly selective slurries might help in avoiding defects such as erosion of sub layers, there still exist planar defects such as dishing, WTWNU due to the differential polishing pressure during the process. The defectivity of micro scratching and particle residue on the surface of the wafer can also arise after polishing.

3.2.4. Agglomeration

3.2.4.1. Mechanics of agglomeration. The ideal slurry will have abrasives crystallized as discrete single particles. However, particles in real CMP slurry apart from being discrete also exist in form of aggregates and agglomerates, as shown in Fig. 46 [65,152,153]. A discrete particle is a single solid sphere or other geometric shape. An aggregate is assembly of multiple particles with strong physical or chemical attachment. Agglomerate is particles and/or aggregates that come together into close-packed

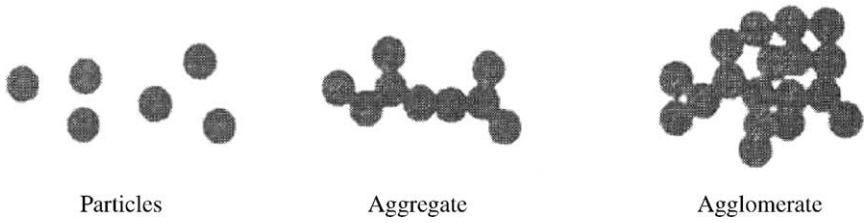

Fig. 46. Three different forms of silica particles [152] (copyright © 1979, reprinted by permission of John Wiley & Sons).

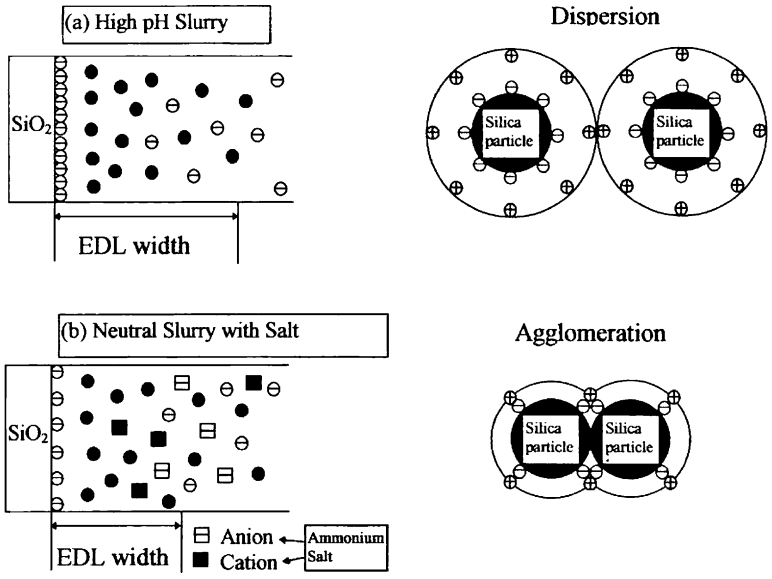

Fig. 47. Illustration of agglomeration mechanism of silica (after Hayashi et al. [154]).

clumps that are not sufficiently ionically charged to provide permanent suspension. These large groups of particles are not desirable for CMP slurry as they can cause micro scratches due to deep indentation or non-uniformity due to differential polishing pressure. The agglomeration phenomenon can be prevented using the techniques of milling at the point of slurry manufacture [65], filtration and proper electrolyte balance. The tendency of the particles to agglomerate is also dependant on the pH of the slurry. The illustration of agglomeration mechanism is shown in Fig. 47. The details of the agglomeration phenomenon can be obtained from literature [154].

3.2.5. Slurry particle effect

The CMP slurry is generally made up of poly-dispersed colloidal or fumed abrasive particles. The particle ideally should have spherical shape; however, anomalies exist in the shape and size of the particles. Recently mono dispersed particles with slender tolerances in shape and size are being used in the slurry to avoid the CMP defects such as dishing and erosion which occur due to uneven polishing. The procedure to synthesize particles with uniform shape and size has been published in literature [155–157]. The effect of slurry particle shape on the removal rate has been studied by Zhenyu Lu et al. Fig. 48 shows the different hematite (Al_2O_3) particles synthesized by Zhenyu Lu et al. The effect of particle morphology on the removal rate during Cu and Ta polishing can be seen in Fig. 49.

3.2.6. Particle less slurry

The abrasive free slurry was developed to overcome of the teething defects such as dishing, erosion, microscratching (discussed in the previous section), Cu and oxide loss and numerous disadvantages of conventional CMP. The removal mechanism, which is predominantly chemical with the mechanical component coming from the polishing pad can be understood by employing electrochemical methods for understanding the role of each chemical component of the slurry. When polished in conventional slurries Cu layer is oxidized by the slurry to form a much harder layer, which is then removed by the abrasive particles and the pad. The abrasive free slurry employs a slightly different mechanism where by the Cu is oxidized in to a corrosion resistant complex, which is much softer than oxide of Cu formed in conventional slurry, and the polishing pad removes the Cu-complex.

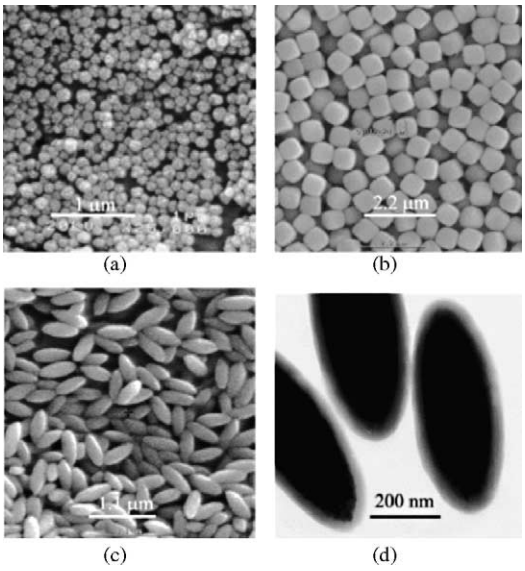

Fig. 48. Electron micrographs of: (a) spherical hematite (α-Fe_2O_3) particles (100 nm in diameter); (b) cubic hematite particles (650 nm in length); (c) ellipsoidal hematite particles (440 nm in length); and (d) hematite particles coated with a 60 nm shell of silica [157].

The comparison of the mechanism of material removal using conventional slurry and abrasive free slurry is indicated in Fig. 50a and b.

In addition to Cu abrasive free slurry, a slurry for second step TaN polishing has also been developed. The prime objective of the TaN is to minimize oxide loss during overpolish as surface deformity is not as much a problem with TaN as it is with Cu due higher hardness of TaN surface. Fig. 51 shows the comparative post-CMP evaluation of patterned Cu wafer polished by conventional slurry and abrasive free slurry. As seen in the schematic, there is a decrease in microscratching, particle residue adherence to the wafer surface, erosion oxide loss and dishing, etc. All in all a much improved performance is shown by the CMP process when abrasive free solution is used [159–162] (Table 8).

The implementation of abrasive free slurry for first CMP step to polish Cu and then second CMP step to polish TaN performed extremely well as can be seen from Tables 9 and 10.

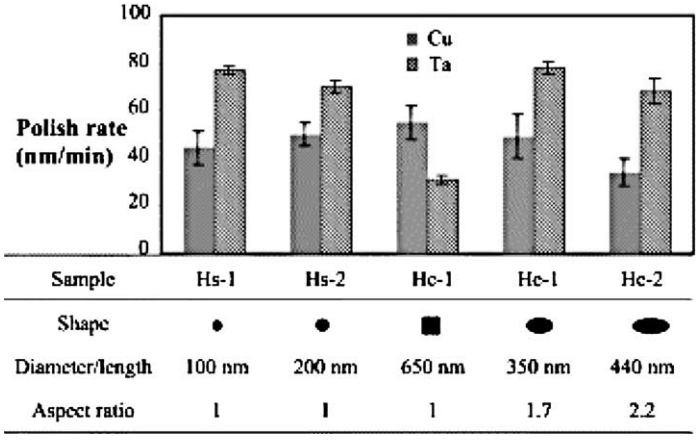

Fig. 49. Effect of slurries of hematite particles of different shapes in dispersions containing 3 wt.% solids and 5 wt.% H_2O_2 at pH 4 on the rate of polishing of Cu and Ta discs [157].

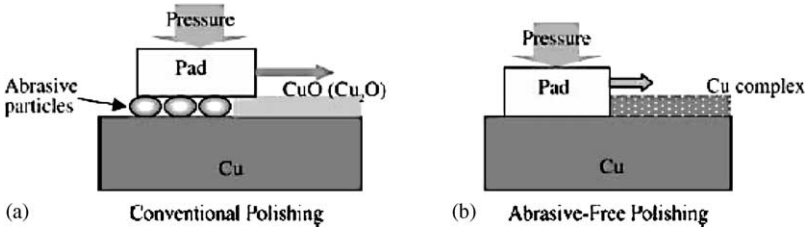

Fig. 50. Comparison between polishing mechanism for: (a) conventional Cu polishing and (b) abrasive free Cu polishing [158].

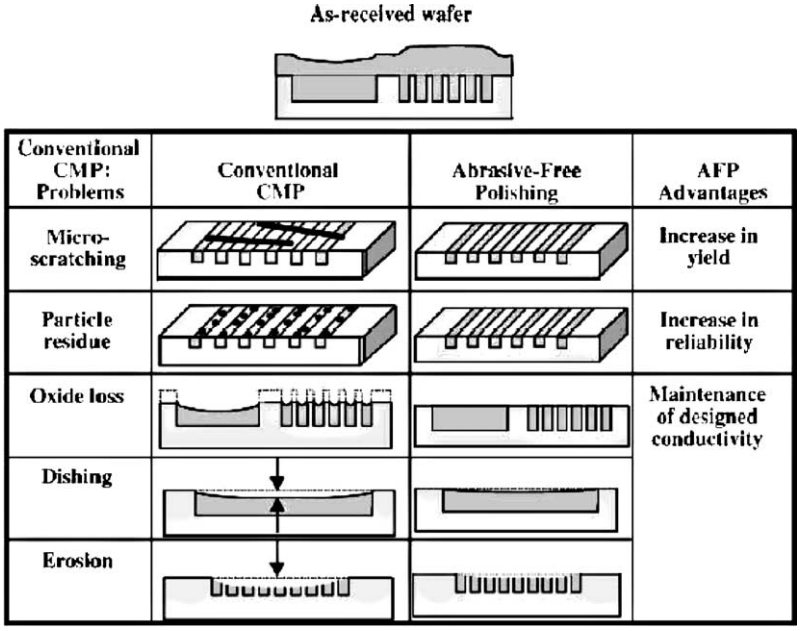

Fig. 51. Advantages of applying slurry free polishing for Cu CMP [158].

Table 8
Polishing rate and surface temperature of the CMP process if different colloids [128]

Slurry	Polish rate range (Å/min)		Process temperature range (K)	
	Low	High	Low	High
3	101.3 ± 44.3	323.3 ± 44.3	300.7 ± 0.5	311.4 ± 0.5
4	76.3 ± 63.5	630.3 ± 63.5	301.5 ± 1.6	314.6 ± 1.6
5	241.7 ± 192.7	1707.3 ± 192.7	304.2 ± 3.5	333.8 ± 3.5
6	476.2 ± 294.2	2949.2 ± 294.2	302.3 ± 2.0	324.1 ± 2.0
7	738.9 ± 422.1	3656.9 ± 422.1	303.0 ± 3.2	326.5 ± 3.2
8a	893.5 ± 245.8	6479.8 ± 245.8	303.8 ± 1.1	334.5 ± 1.1
8b	256.9 ± 91.6	487.8 ± 91.6	304.4 ± 2.5	316.1 ± 2.5
8c	28.9 ± 13.4	70.6 ± 14.2	303.2 ± 1.7	340.9 ± 1.8

Table 9
Performance of abrasive free slurry on 8 in. Cu wafer [158]

Items	Values
Removal rate (Å/min)	
Cu	5500
TaN	<1
Selectivity (Cu/TaN)	>5500
Micro-scratch (<0.2 μm)	10v
Dishing (L/S = 100/100 μm, 50% density) (Å)	500
Erosion (L/S = 1/0.5 μm, 67% density) (Å)	150

Table 10
Performance of abrasive free slurry on 8 in. TaN wafer [158]

Items	Values
Removal rate (Å/min)	
Cu	150
TaN	1000
SiO_2	20
Selectivity	
TaN/SiO_2	50
TaN/Cu	7
Cu/SiO_2	7

3.2.7. Slurry rheology studies

CMP slurries are mostly complex mixtures of water, alkali or acid, abrasives, additives for specific purposes, which may or may not physically or chemically interact with each other. The slurry properties are highly sensitive to slurry chemistry, temperature as well as the effect of shearing during delivery [105]. As a result of shearing agglomeration of particles might occur in the slurry solution [163]. Viscometry tests which determine viscosity at a particular temperature in steady-state mode have been previously used to determine the changes in the slurry due to shear. In order to characterize the effect of shearing on slurry properties, Moinpur et al. have applied dynamic rheometry tests. In the steady-state measuring mode, dynamic rheometry measures viscosity at a wide range of shear rates and temperatures. Additionally, in the frequency-sweep mode, it determines the dynamic-shear storage (G') and loss (G'') moduli, tangent of mechanical losses (tan δ), and complex viscosity ($\eta^* = \eta' - i\eta''$). The time-sweep mode measures viscosity changes under constant shear over a period of time. The temperature/frequency-sweep mode allows prediction of time and temperature dependant slurry properties using time–temperature superposition principle. Thus dynamic rheometry is a powerful technique to better understand the mechanical and chemical aspects of the CMP slurry [164].

An example of a frequency-sweep test of slurries at two different temperatures (5 and 30 °C), is shown in Fig. 52. As slurry temperature increases dynamic shear storage and complex viscosity decrease. Transient changes in slurry can cause defects on an intermittent basis. The measurement of transient viscosity, viscosity changes and their impact on CMP have been discussed by Lortz et al. The authors also give the details of the experimental set up for measurement of slurry viscosity. In depth analysis of slurry viscosity explains the non-Newtonian behavior of the slurry at some instances during the CMP process [165].

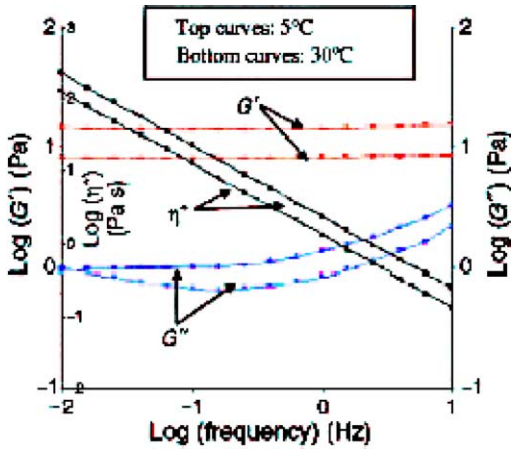

Fig. 52. Frequency-sweep test for two different temperatures [105].

3.3. Slurry application

For the purpose of convenience the CMP slurries are further categorized in to three classes: (1) oxide slurries; (2) metal slurries; (3) STI slurries.

3.3.1. Oxide slurry

The most commonly used abrasives in CMP slurries are silica (SiO_2) and alumina (Al_2O_3). The physical appearance of these abrasives, before mixing with water, is white powders. These materials must be ultrapure (>99%) and have nearly uniform particle shape and size to ensure a consistent and reasonable polish rate.

3.3.2. Abrasives for oxide slurry

Commercially silica is used in oxide CMP slurries. The size of an abrasive particle is in the range of 500–2000 Å. The fumed silica is formed by oxidizing chlorisilane ($SiCl_4$) in a flame reaction at 1800 °C [65].

$$SiCl_4 + 2H_2 + O_2 \rightarrow SiO_2 + 4HCl$$

In contrast to fumed silica, colloidal silica is synthesized in the liquid phase. The starting material is sodium silicate (Na_2SiO_3), or sometimes the sodium *meta*-silicate ($NaHSiO_3$), which are liquid glasses with approximately 70% SiO_2. By mixing liquid glass and water, colloidal silica crystals will be formed and suspended simultaneously. The material is then stabilized by passing it through an acid (H^+) charged ion exchange resin. As a result, the shape of the colloidal silica particle is spherical. The typical particle distribution of in silica slurry is seen in Fig. 53a and b.

3.3.3. Abrasives for metal slurry

Unlike oxide slurries, which use only one kind of abrasive (silica), metal slurries use various types and mixtures of abrasives. Another factor is that the solution (oxidizer) in metal slurry plays a more dominating role. As a result, to obtain the desired polishing performance, the selection of the oxidizer outweighs the selection of abrasives in importance. After a metal oxidizer has been selected, the type and the size of the abrasives must fit in. Alumina is the most often used abrasive in tungsten slurries.

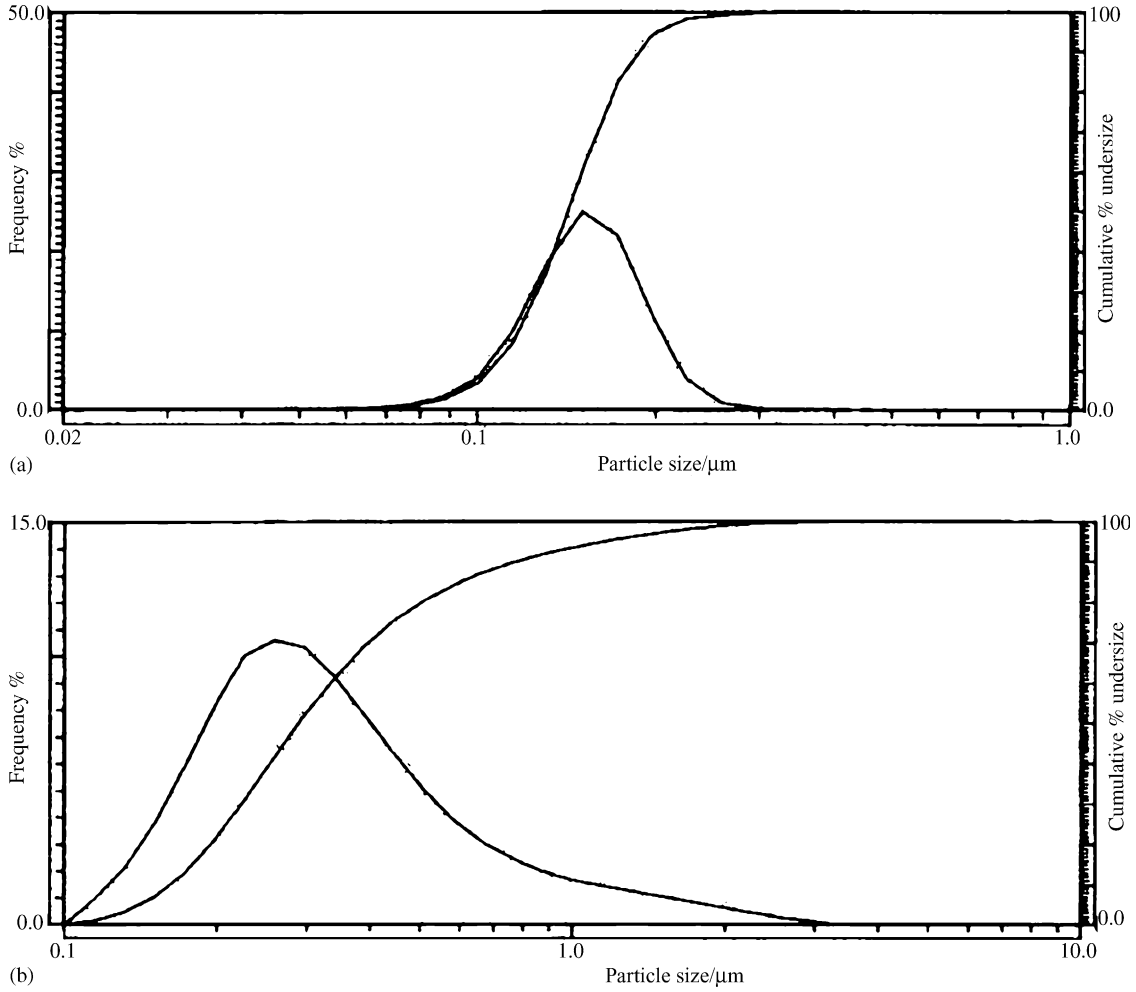

Fig. 53. Typical particle size distribution of silica in oxide CMP slurry: (a) normal and (b) abnormal with a long tail [65].

The ammonium alum ($NH_4Al(SO_4)_2H_2$) is precipitated by the mix of two solutions, namely, aluminum sulfate ($Al_2(SO_4)_3$) and ammonium sulfate ($(NH_4)_2SO_4$). After precipitation, the precipitated alum is collected and calcinated. The ammonium alum will be converted into pure ammonia. Depending on the completion of the phase change kinetically, the alumina can be either gamma or alpha phase. Alpha phase alumina is harder than the gamma phase [65].

3.4. Slurry solution

The slurry solution plays a different role in oxide (as a hydrolizer) and metal (as an oxidizer) slurries.

3.4.1. Solution for oxide slurry

Fumed and colloidal silica slurries are predominantly used for oxide polishing. The slurry solution for oxide slurry is mainly KOH or NH_4OH based with pH $>$ 10. NaOH slurry is the best

medium of OH^- ion, however, as Na^+ is notoriously mobile, there is a possibility that it can cause contamination of the device lying under the interconnect structure. Though the K^+ ion is not as mobile as the Na^+ ion, it can easily getter through BPSG. For this purpose the preferred oxide slurry is one, which is based on NH_4OH and has colloidal silica.

3.4.2. Solution for metal slurry

On one hand, the selectivity between different metal layers should be close to unity. On the other hand, the selectivity between metal and oxide should be as large as possible. Further, on one hand, the polish rate for metal needs to be higher than 3000 Å/min, on the other hand, dishing or plug recession must be minimized at the metal areas on the patterned wafers. Currently, there are four different commercial tungsten slurries; namely, $Fe(NO_3)_3$-based, H_2O_2-based, KIO_3-based, and H_5IO_6-based slurries. Briefly speaking, the $Fe(NO_3)_3$-based, the KIO_3-based and the H_5IO_6-based oxidizer will dissociate into cations and anions (with different NO_x and IO_y complexes), and the anions will oxidize tungsten. In contrast, an H_2O_2-based slurry decomposes into H_2O and dissolved O_2, and the O_2 directly reacts with tungsten. In general, the oxidizing ability is in the order of: $H_2O_2 > Fe(NO_3)_3 > H_5IO_6 > KIO_3$ [65].

3.4.3. Solution for tungsten slurry

The H_2O_2-based slurry performed the best in slurry evaluation. However, it has problems with plug recess and field oxide erosion. The pot life has also been previously compared among the H_2O_2-based, the Fe $(NO_3)_3$-based, and the H_5IO_6-based slurries after mixing the abrasives (suspended in water). It has been found that Fe $(NO_3)_3$-based slurry can last the longest (more than 6 months) without significantly losing polish rate. The H_5IO_6-based slurry slightly loses its polish rate. However, the H_2O_2-based slurry looses 50% polish rate in 100 h. This indicates the poor stability of the slurry. The H_2O_2 decomposes and the dissolved O_2 evaporates in a short period of time. Therefore, to run the H_2O_2-based slurry, in situ mix and/or auto-titration are required [65].

3.5. Chemical mechanical polishing pads

CMP is a complex interplay between the wafer and the consumables involved. As discussed earlier in this section, the different slurry parameters dominate the CMP process behavior. The CMP polishing pad is the other consumable which also has an equally dominating effect on the CMP process output. One such CMP consumable, where there is extensive scope for development and improvement, in order to meet the ever-increasing process reproducibility and reliability demands of the semiconductor industry, is the CMP polishing pad. The polishing pad is made up of a matrix of cast polyurethane foam with filler material to control hardness of polyurethane impregnated felts. The pad carries the slurry on top of it, executes the polishing action, and transmits the normal and shear forces for polishing, there by playing a very crucial role in process optimization [56,166–169]. Polyurethanes have a unique property of combining high strength and high hardness and modulus combined with high elongation at failure. A stacked pad consisting of an IC 1000 top layer on a Suba IV sub-pad (Rodel Inc., Newark, DE) is currently the pad system of choice to obtain both good global wafer uniformity and small step heights (Fig. 54).

3.6. Pad classification

The pads used in semiconductor manufacturing can be grouped in four classes: class I, felts and polymer impregnated felts; class II, microporous synthetic leathers; class III, filled polymer films;

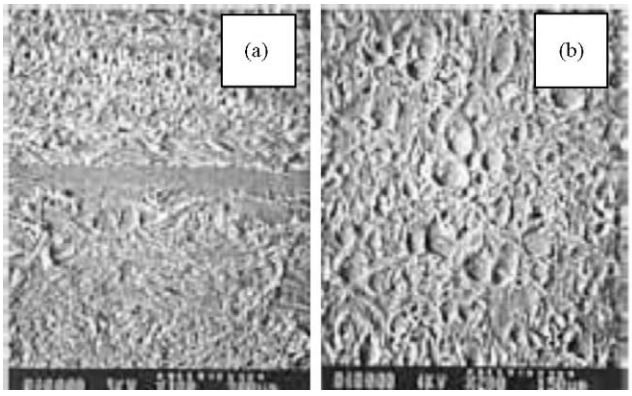

Fig. 54. (a) Scanning electron micrograph (SEM) of cross-section of IC 1000 B4/Suba IV pad and (b) SEM of the surface of IC 1000 [169].

class IV, unfilled textured polymer films. The summary of pad classifications and their properties are given in Table 11.

3.7. Effect on pad manufacturing process

The different processes involved in fabrication of the polishing pad have been detailed elaborately in the literature [65]. The different process steps involved in pad manufacture to imbibe certain properties in the pad have direct effect on their mechanical properties. Table 12 shows the effect of different manufacturing processes on the pad properties.

3.8. Effect of temperature change on polishing pad

The polishing pad might be subjected to elevated temperature during the course of the CMP process. The heating is due to the frictional forces generated when there is solid–solid contact during the polishing [103]. The solid–solid contact can cause local heating of the pad up to 30 °C [105]. There is some alleviation of heating when the polishing is done in hydrodynamic contact mode [103]. However, there is overall increase in the pad temperature irrespective of the mechanism of polishing. The effects of pad heating are compounded if the chemical reaction between slurry and pad is exothermic [65]. The mechanical, physical and chemical properties of the polyurethane material can be permanently or temporarily altered if the pad is heated beyond a particular limit [170]. Several tests such as dynamic mechanical analysis (DMA), thermomechanical analysis (TMA) and thermogravimeteric analysis have been performed for material characterization of the polishing pad. This subsection elaborates on some of the pad thermal characterization tests, procedures and results.

3.8.1. Dynamic mechanical analysis

The applicability for DMA for polishing pads has been elaborately studied by Lu et al. [103]. Based on the results of previous experiments performed by Li et al. [171] DMA was performed to evaluate the structure–property relationship of polyurethane pad. The change in tan δ curve of the DMA spectra can show changes in the glass transition temperature (T_g) of a stacked pad. The glass transition temperature is the temperature at which the macromolecules of the polyurethane breakaway form entanglements and undergo micro-Brownian motion [172]. Investigation of glass transition temperature of the polyurethane pad is important as it corresponds to sharp decrease in hardness and

Table 11
Summary of polishing pad classes [65]

	Class I	Class II	Class III	Class IV
Major structural characteristic	Felted fiber with polymer binder	High-porosity film on substrate	Solid urethane sheet with filer (voids, SiO_2, CeO_2, etc.)	Solid polymer sheet with surface texture
Subcategories	Spun bond nonwovens	Free-standing thin films; felt substrates	Foams; oxide filled	
Hardness	Medium to high	Low	High	Very high
Compressibility	Medium to high	High	Low	Very low
Slurry carrying capacity	Low to high	Very high	Low	Minimal
Bulk microstructure	Continuous channels between fibers	Complex foam to vertically oriented channels	Closed cell to open cell foam	None
Polymer types employed	Urethanes; polyolefins (fiber phase)	Urethanes; polyolefins (fiber phase)	Urethanes	Various
Representative commercial trade names	Pellon™, Suba™	Politex™	IC 1000	OXP3000
Application(s)	Si stock polish; tungsten damascene CMP	Si final polish; metal damascene CMP; post-CMP buff	Si stock; ILD CMP; metal dual damascene	ILD CMP; shallow trench isolation; metal dual damascene

Table 12
Manufacturing process variables and their effects on pad properties [65]

Process	Variables	Effects
Felting (web)	Fibersize	Composite modulus
	Particle density	Volume fraction for impregnation polymer; composite modulus; hardness; liquid permeability
	Random vs. nonrandom fiber orientation	Anisotropy of physical properties
Impregnation (web)	Polymer type	Composite modulus; hardness; viscoelasticity
	Volume fraction	Composite modulus; hardness; liquid permeability
	Microstructure	Composite modulus; hardness; liquid permeability
Coating (web)	Pore dimension	Composite modulus; permeability
	Coating height	Composite modulus; permeability
	Random vs. non random	Anisotropy of physical properties
	Porosity	
Scuffing (web, batch)	Removal depth	Pore dimension; coating height
		Surface roughness
	Abrasive size	
Casting (web)	Polymer type	Hardness; modulus; viscoelasticity
		Composite modulus; liquid permeability; surface roughness
	Filler size	Composite modulus; liquid permeability; abrasivity
		Modulus; hardness; viscoelasticity
	Filer volume fraction	
	Thermal history	
Texturing (web, batch, net)	Texture dimensions	Liquid permeability; pad hydrodynamics
Contaminating (web, batch, net)	Member thickness	Composite materials
	Property changes due to processing	Modulus; surface roughness; liquid permeability

modulus of the pad which in turn affect the removal rate and global planarization. The methodology and experimental set up of DMA has been discussed elaborately by Lu et al. [103].

Fig. 55 shows the storage modulus of a new stacked IC 1000/Suba IV stacked pad when the temperature sweep was fixed at 125–200 °C as shown by Li et al. It can be seen from the figure that Suba IV had lower storage modulus as compared to IC 1000. The lower rigidity of Suba IV can be attributed to composition of a polyurethane coating that contained a chain extender. The overall contribution of the stiffness of the pad is a combination of individual components of the rigidity of each of the components of the stacked pad including the pressure sensitive adhesive (PSA). Hence the storage modulus of IC 1000 most closely matches the storage modulus of the IC 1000/Suba IV stacked pad as IC 1000 has a higher relative functional contribution.

It is also interesting to compare the mechanical properties of an unused and used pad and study the effect of pad degradation on storage and loss modulus. Lu et al. [103] have shown comparative E' and tan δ curves of an unused IC 1000/Suba IV stacked pad and another IC 1000/Suba IV that is near to the end of its polishing life. It can be seen from Fig. 56 that storage modulus of the used pad is

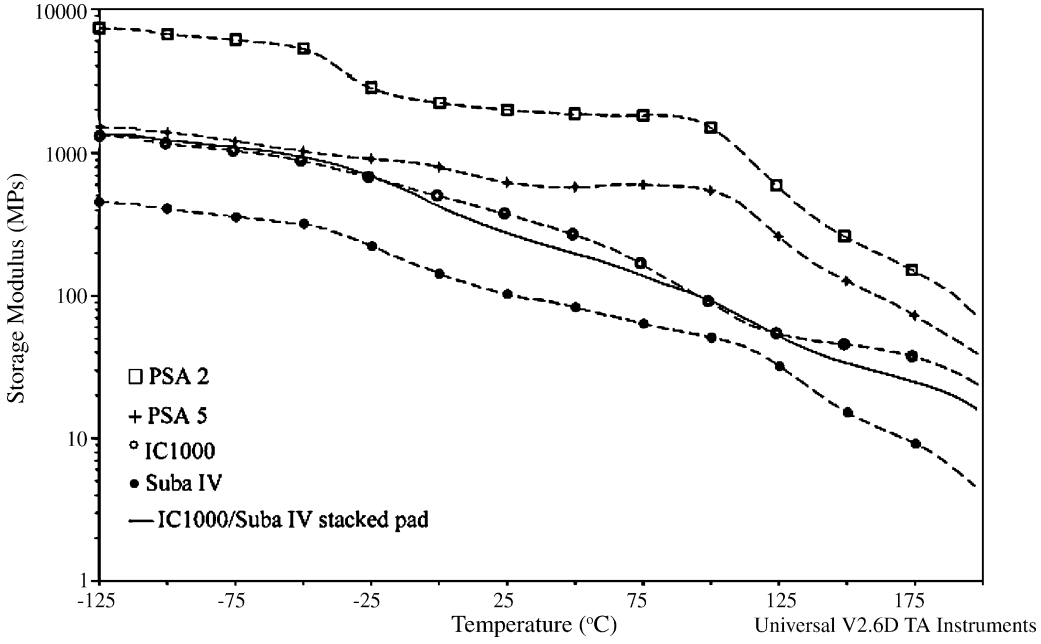

Fig. 55. A storage modulus (E') comparison between stacked pad and its components [103].

considerably lower than that of the new pad at temperature below 0 °C, is comparable between 0 and 40 °C and then goes on to increase above that temperature.

The T_g of the polishing pad is affected by the number of chemical and molecular aspects. The T_g peak as shown by Lu et al. shifted to a higher temperature and was considerably broader for the used

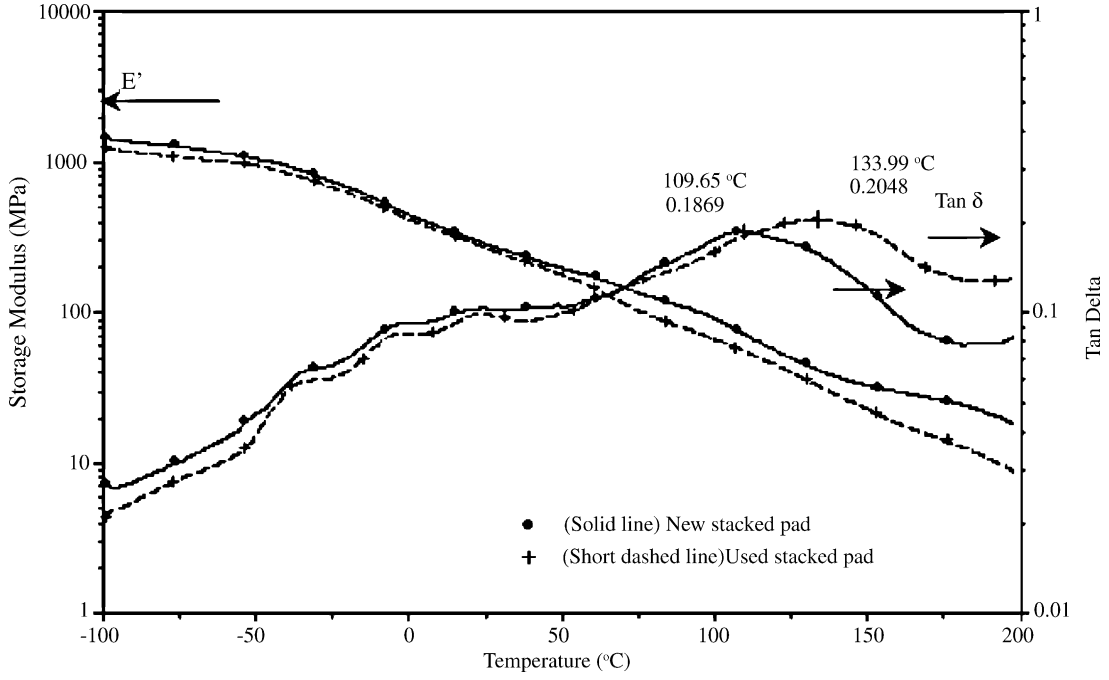

Fig. 56. Storage modulus (E') and tan δ differences between new and used pads [103].

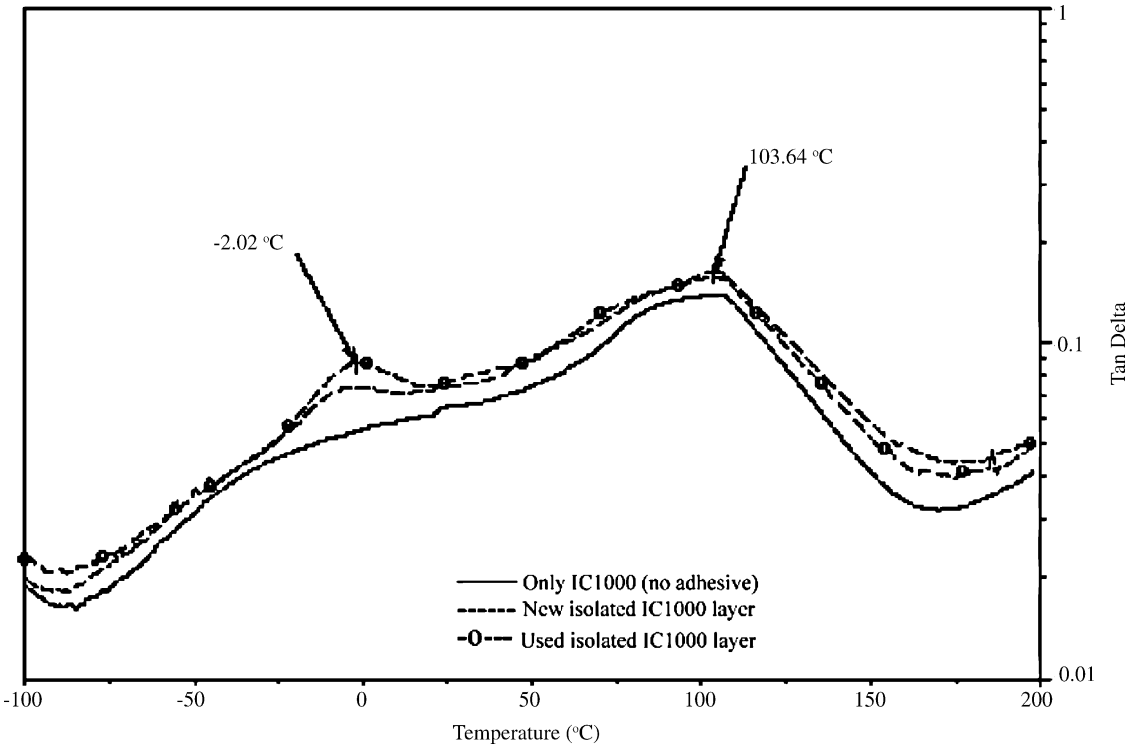

Fig. 57. Tan δ overlay curves between isolated new and used IC 1000 layers [103].

pad as compared to the new pad. During CMP the top part of IC 1000 comes in contact with the alkaline slurry. Hence, Lu et al. isolated the top layer of IC 1000 to study the pad degradation during CMP process. Fig. 57 showed the relative variation of new and used isolated IC 1000 layer and IC 1000 layer without adhesive.

Lu et al. attributed the upward shift also to the degradation of IC 1000 when used and the decrease in their relative component in the composite pad. Assuming the pads obeyed the copolymer equation

$$\frac{1}{[T_g]_{\text{stacked pad model}}} = \frac{X_a}{[T_g]_{\text{IC 1000}}} + \frac{X_b}{[T_g]_{\text{Suba IV}}} \tag{3.4}$$

and as $X_a + X_b = 1$, it can be inferred that

$$[T_g]_{\text{stacked pad model}} \propto \frac{1}{X_a} \tag{3.5}$$

The hypothesis of the increase in glass transition temperature with decrease in the thickness and hence the relative component of the IC 1000 pad due to degradation has been conclusively proven by Lu et al.

3.8.2. Thermo mechanical analysis

The coefficient of thermal expansion of the pad below 25 °C and above 50 °C was monitored by Moinpur et al. using the thermomechanical analysis as shown in Fig. 58. The lower limit temperature is shown as T_{low} and higher limit temperature is shown as T_{high} in the figure. Moinpur et al. propose that it is advisable to operate the pad in the temperature range where the coefficient of thermal expansion is zero and the pad does not exert pressure on the wafer. The in order to get a wide window for pad

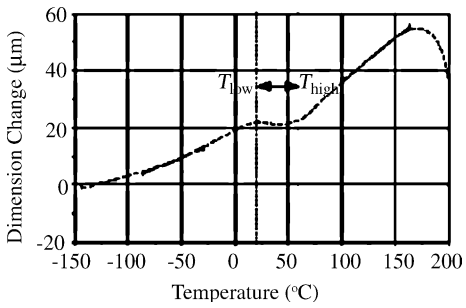

Fig. 58. Thermomechanical analysis (TMA) scan for a CMP pad conditioned at room temperature and tested using penetration microprobe [107].

operating temperature, the pad is annealed at different temperatures for different times. It was observed that proper thermal treatment allows the pad to operate at an amicable temperature and thus achieve desired processing results. The details of pad annealing are available in literature [105].

3.9. Non-uniformity of the polishing pad

The pad might be directly responsible for several process defects like WTWNU where there is non-homogeneity of polishing when one wafer is compared to another or within wafer non-uniformity (WIWNU) where there is non-homogeneity of polishing at different areas of the same wafer. In order to improve the yield of the CMP process, to get a highly planar defect free uniform wafer surface and to reduce the overall manufacturing costs involved, there is a need to extensively study the fundamental properties of the CMP pads on the whole.

The scanning ultrasound transmission (UST) is a nondestructive technique developed that works on the principle of ultrasound permeability through absorbing visco-elastic medium [103]. The difference in the ultrasound absorption in the areas of varying density and viscoelasticity is used to determine the non-uniformity within a single pad there by giving an in depth idea of the physical characteristics of the given pad. Fig. 59 shows the set up of the UST equipment. The details of UST are available in literature [170].

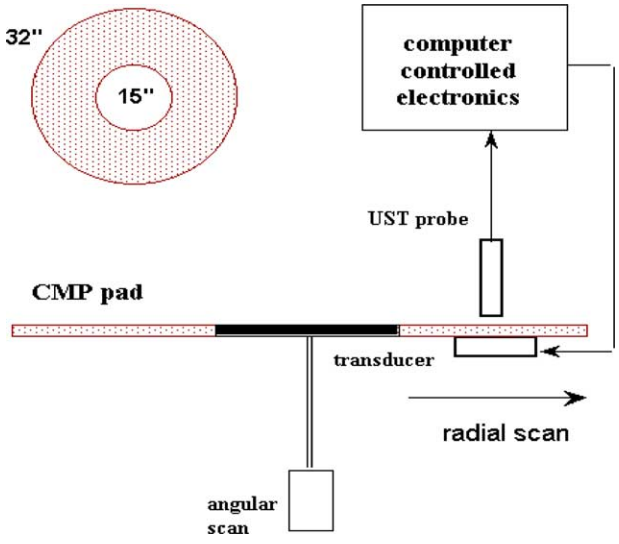

Fig. 59. Schematic of USF system [170].

The full map image of the pad was obtained with the UST system using linear and rotary stages driven by step motors with 7 mm radial and 2° angular resolutions. After the mapping, 6 in. diameter coupons were punched out of the area seen to be non-homogenous as well as homogenous pad area. The pad was then re-mapped after pressing the coupons in place from where they were punched in the first place. The effect of the procedure on the homogeneity of the pad was observed.

DMA was performed on the 20 mm × 10 mm samples cut from the 6 in. diameter coupon punched from the pad. The experiment was performed keeping the temperature increments of 4 °C with an isothermal time of 1 min per increment over a range of 30–80 °C (room temperature). The flexural mode was used with single cantilever clamp and 3.0 μm amplitude. The frequencies for the run ranged from 0.6 to 100 Hz. The set up and working of DMA is already well established [103,171].

Fig. 60a shows the results of the complete 360° scanned ultrasound mapping of IC 1000/Suba IV dual pad. It can be noted that the pad has a distinct region of high and low ultrasound transmission [173]. Two, 6 in. coupons (denoted by circles drawn on the full scale scan) of the pad were punched from the low and high ultrasound transmission regions. After punching, the pad was remapped placing the coupons at the same positions on the pad. The results of the area scans of coupons replaced in the original position are shown in Fig. 60b and c. It can be seen from Fig. 60b that the ''high-intensity'' coupon (#A) after punching and remapping showed reduced ultra sound signal transmission as compared to the surrounding pad and the previous magnitude of ultra sound signal transmission. This indicates that high-UST region in the full map corresponds to the compressed part of the pad material (pad is under compressive stress), which is relaxed when coupon was punched. It can be estimated that 20% variation of the UST

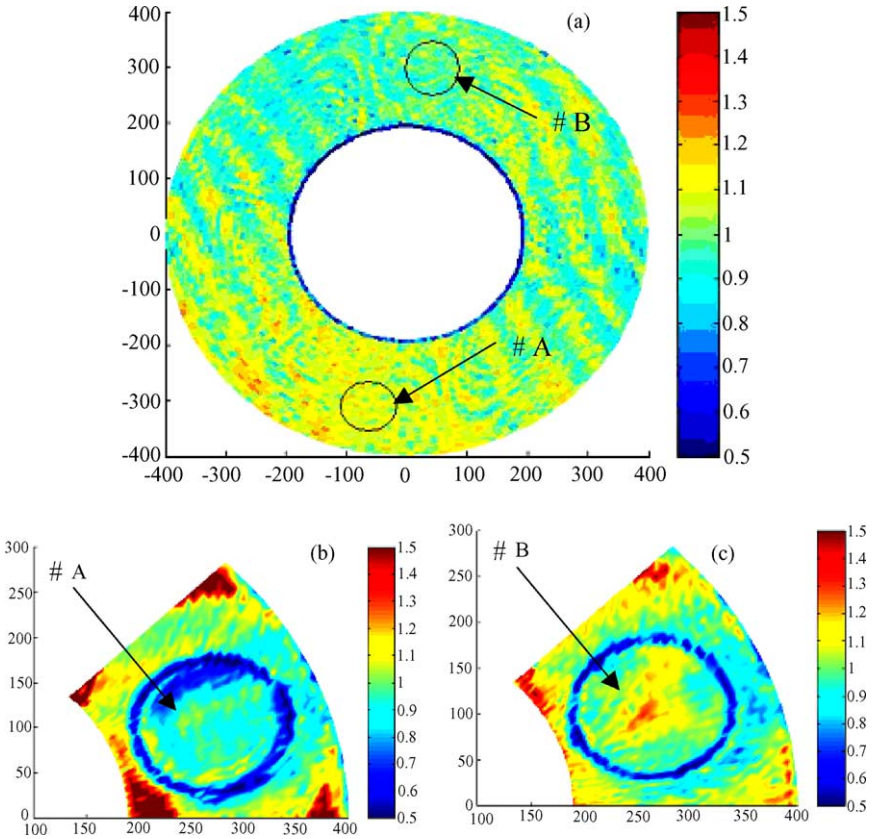

Fig. 60. (a) Pad mapped before punching 6 in. coupons; (b) areas of high intensity mapped (coupon #A); and (c) area of low intensity mapped (coupon #B) (all the values have been normalized over the entire area) [103,171,174].

amplitude between high and low intensity areas corresponds to 10% relative change of the pad density (specific gravity). It has to be emphasized that this local density variation has to be assessed on the whole pad and not on the coupons due to stress relaxation. The distinct lower signal at the edge of the coupon in Fig. 60b and c shows that there is an air gap between the punched coupon and the entire pad at the edge of the coupon. Certain distinct areas of reduced ultra sound signal transmission in the coupon showed in Fig. 60b also indicate that there is an air gap underneath the coupon when it is put back in place. The coupon shown in Fig. 60b is not able to take the original flat shape after being punched.

When the coupon from lower UST intensity (#B) is punched and remapped after placing it in its original position, as seen in Fig. 60c, the edge of the 6 in. coupon shows decreased ultra sound signal transmission similar to #A coupon (Fig. 60b). Even in this case, there exists an air gap at the edge of the coupon. However, the coupon shown in Fig. 60c remains flat in the position when replaced at the original position after being punched. The ultra sound signal over the entire coupon remains more or less the same as seen in the previous scan (Fig. 60a). However, there is an increase in the UST amplitude in the center of this coupon suggesting that certain regions of the ''lower intensity'' area of the pad were under tensile stress and after being punched relax, which makes them denser, thus increasing the UST signal.

Dynamic mechanical analysis (DMA) was performed on pieces of the coupons punched out of the pad. Fig. 61a shows the comparison of the variation of the storage modulus with temperature of pad material measured from low and high intensity regions. Even though there is a difference in the value of storage modulus of the material measured from the ''high intensity'' and ''low intensity'' region at 100 Hz frequency and 30 °C, as the temperature increases, the values of the storage modulus of the pad material from both high and low intensity regions are very close and show similar trends.

The trend of variation of the storage modulus for both samples is very similar or identical for the 30 and 0.6 Hz. It can be seen in Fig. 61b, that there is no significant difference between the values of loss modulus for the compared samples at 100, 30 and 0.6 Hz. The curves of variation of the loss modulus with temperature for all the measured frequencies followed similar trends. Fig. 61c shows the variation in tan δ parameter with frequency at different temperature for the compared materials. The values of tan δ at different measured temperature and frequencies occur in close proximity and the variation even in the case of tan δ shows a similar trend [174]. As the pad is made up of the same homogenous polyurethane material, there is no difference between the mechanical properties of the samples taken from the ''high intensity'' and ''low intensity'' regions. The experiment was repeated for verification of the trend obtained from an earlier experiment.

Previously, similar experiments were performed with the same commercial IC 1000/Suba IV. One and three inch coupons were cut and placed again, remapped and analyzed using DMA, similar results were found even in that case. The set of experiments when repeated on other polyurethane pad showed that there is no variation in the bulk material properties of the material taken from the high and low ultra sound transmission regions. The coupons of high intensity and low intensity regions were evaluated for their tribological properties using the CETR CMP tester discussed in the previous section. Fig. 62 shows the variation of COF at different rpm when thermally grown 3000 Å SiO_2 is polished using the high and low transmission pads at 3 psi down force. There is no significant trend in the variation of COF of the regions belonging to high and low transmission regions in the pad.

Thus it can be inferred that there exist high and low transmission regions, i.e. high and low specific gravity regions in the pad presumably due to the variations in the pressure sensitive adhesive. The regions can cause non-uniformity in the wafer. However, attempts to isolate these regions will be futile as the variation is due to the built in stresses which are released when the coupons are isolated from the polishing pad. To accurately gage the effect of these specific gravity regions, a mechanism of localized polishing of the pad needs to be developed and results need to be studied [175,176].

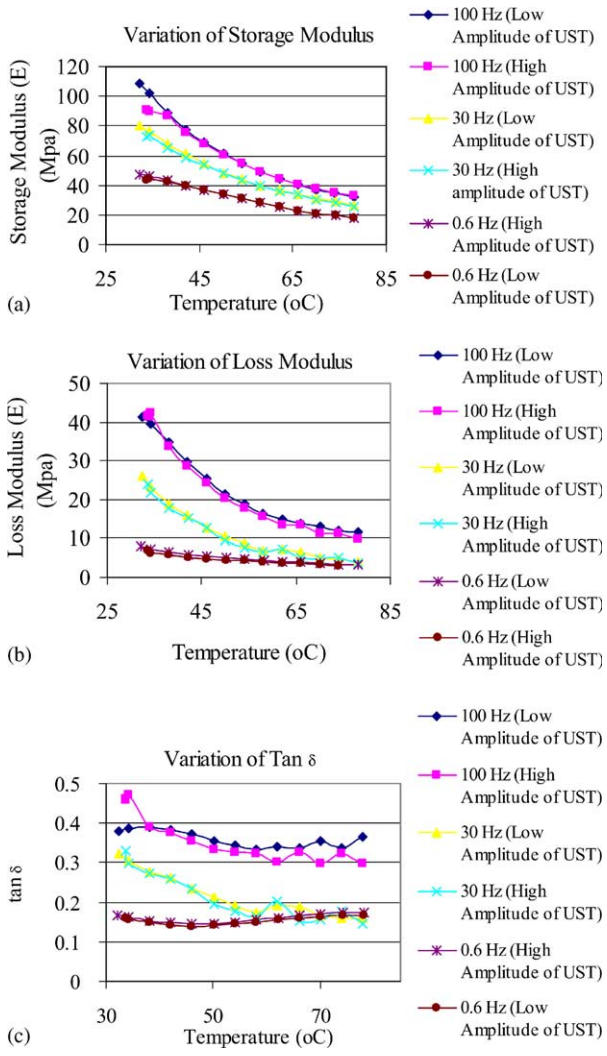

Fig. 61. (a) Variation of storage modulus vs. temperature; (b) variation of loss modulus vs. temperature; and (c) variation of tan δ vs. temperature of samples tested from low and high intensity region of the pad [172,173].

3.10. Dishing and erosion polishing defects

Since surface topography of the wafer after the CMP process determines the device yield, the dishing of dielectrics and erosion of metal lines has been studied in detail. Dishing and erosion are controlled by the local pressure distribution between features on the surface of the wafer. The difference in pressure on certain features of the wafer can be the result of pad non-uniformity, high pad surface roughness and stiffness. Thus along with the pattern density, line width, applied down force, selectivity of the slurry, the pad properties also need to be accounted for when dishing and erosion studies are performed. Efforts to predict dishing, erosion and compromise in topography have been made since 1991. Warnock performed more of a phenomenological study to model dishing and erosion without going in to the details of the mechanics involved there in [177].

Vlassak [178] has presented the contact mechanics model to predict the extent of dishing and erosion for a particular CMP process step and elucidate the mechanism of dishing. When the pad is

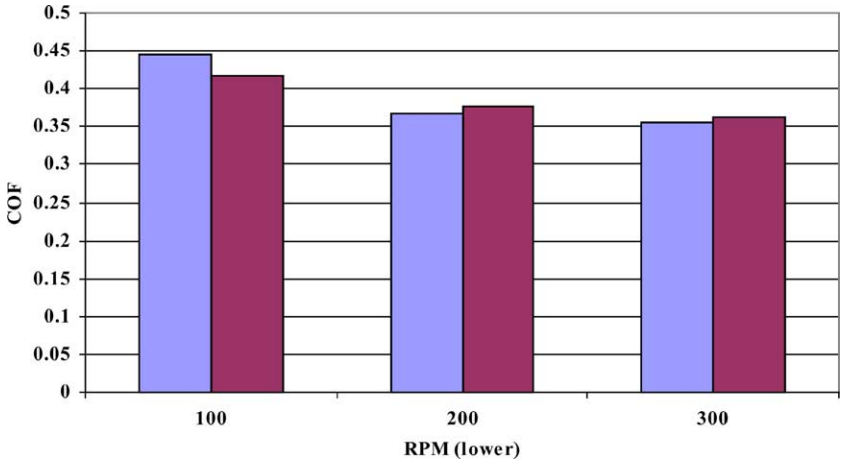

Fig. 62. Variation of COF at different rpm for SiO_2 polished at 3 psi [176].

pressed with a patterned wafer, the asperities come in contact with the wafer and the pad is compressed under the down force of the wafer. Vlassak et al. proposed that the height of the pad asperity can be calculated as

$$P(z) = \frac{1}{2\sigma}\exp\left(-\frac{|z|}{\sigma}\right) \tag{3.6}$$

where z is the height of asperity above and below the pad surface and σ is a roughness parameter that represents the width of asperity height distribution. If $T_{(x,t)}$ function describing the surface profile of the wafer at the given time t, $w_{(x,t)}$ represents the shape of the deformed pad and $d_{(x,t)}$ represents the gap between the wafer and pad. Schematic and free body of a compliant pad during CMP can be seen in Fig. 63a and b [178].

Substituting the various input parameters and boundary conditions, the equations for pressure distribution and pad deformation can be obtained [178]. Knowing the pressure distribution the removal rate can be calculated using Preston's equation [99]. The contact pressure can be estimated utilizing the contact mechanics models by Greenwood and Williamsson [179], and Johnson [180]. Numerical simulation and iteration of the obtained equation as shown by Vlassak et al. can be used to determine the various output parameters of the CMP process at different values of time. Fig. 63a and b shows the variation of the depth of dishing with increasing line width for given values of pattern density, pad stiffness and pad surface roughness factor. It can be seen that there is an increase in dishing with the same pad with increase in the line width and increasing in polishing time (especially crucial when the wafer is over polished). The effect of pattern density on erosion of metal lines can be seen in Fig. 63c and d. The erosion of metal lines increases with increase in polishing time (overpolish) and increase in pattern density. Thus the polishing pad along with time of polish and surface roughness factor play a crucial role in the dishing and erosion CMP process defects.

3.11. Effect of pad grooves

The effect of pad texture on tribological and kinetic properties of polishing pad has been studied by Philipossian and Olsen [181]. Real time monitoring of COF was done to estimate the normal shear forces originating during a particular CMP processes for a given pad. Frictional and removal rate data were taken on Rodel IC 1000 flat, perforated, XY- and K-grooved pads. The details of the experimental

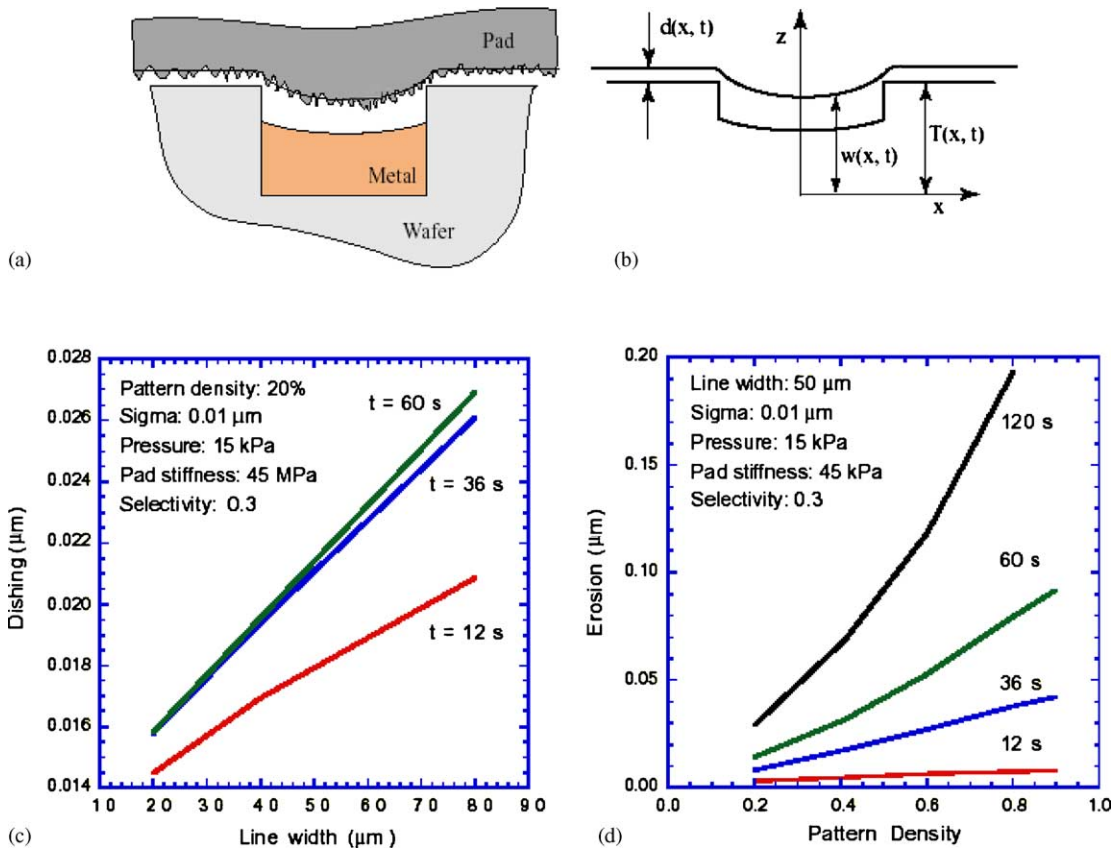

Fig. 63. (a) Schematic; (b) free body diagram of a compliant pad during CMP; (c) variation of dishing with line width; and (d) variation of erosion with pattern density of the polished wafer [178].

set up and parameters can be obtained from literature [181]. The Somerfeld number, COF, a new parameter called tribological mechanism indicator (TMI) and materials removal rate were some of the parameters monitored during the experiments by Philipossian and Olsen.

Philipossian and Olsen reported that (Fig. 64), for a slurry concentration of 2.5%, the Stribeck curve shows that mechanism of polishing for the K-grooved pad remains in boundary lubrication throughout the range of parameters studied. Flat and XY-grooved pads begin in boundary lubrication and migrate to partial lubrication as Sommerfeld numbers increase. Perforated pads begins by exhibiting boundary lubrication and then transition to partial lubrication at higher values of Sommerfeld number. Thus different pad surface texture showed different material removal mechanism. The different removal mechanisms naturally produce different tribological properties, and different removal rate.

After the investigation of the different removal mechanisms and polishing performance of the different grooves on the pad, the effect of grooves on the mechanical properties of the pad must be investigated. DMA of the rectangular samples of polishing pad was performed by Moinpur et al. with a temperature range of −120 to 180 °C, to evaluate the elastic modulus (G), storage modulus (G') and damping properties of pads with different grooves. The effect of pad groove orientation on the storage modulus of the pad is shown in Fig. 65.

The pads with longitudinal groove and grooves in 30 °C show higher storage modulus in the temperature range of −120 to −75 °C. On a macro scale during a CMP process, the effect of difference

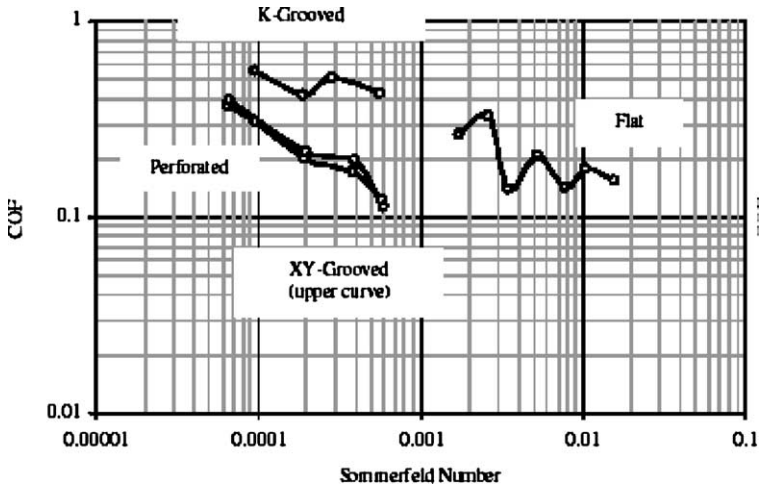

Fig. 64. Stribeck curves for various pad textures for 2.5 wt.% fumed silica slurry [181].

in storage modulus might not produce any significant defects or damage, however, the variation of the mechanical properties need to be studied further on a micro scale to gage its impact on the CMP process and material removal mechanism which is seen to be different from the study of Philipossian and Olsen.

3.12. Physical and chemical changes in pad during polishing

The quantitative analysis of the physical and chemical changes that occur in the polishing pad during polishing was performed by Lu et al. [103]. The surface of the polyurethane pad has been studied and reported in literature [171]. In their research Lu et al. studied the effect to polishing cycles on the pore size and shape of the commercially available IC 1000/Suba IV polishing pad. Fig. 66a and b shows the SEM of the polishing pad before and after polishing, respectively, as shown by Lu et al. [103].

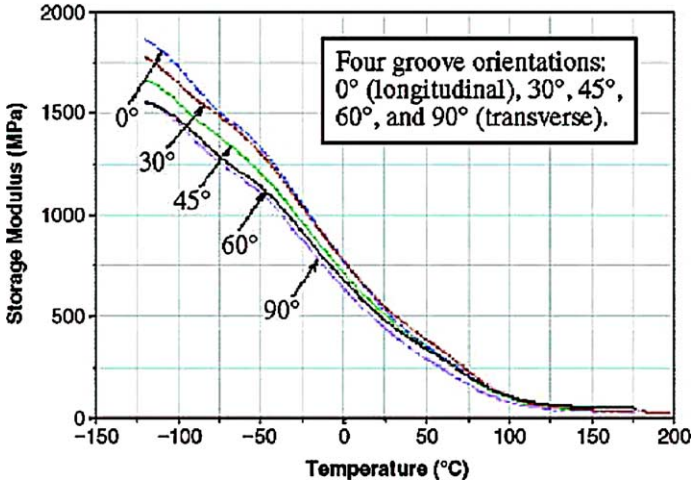

Fig. 65. Dynamic mechanical analysis of pads with different groove orientations [103].

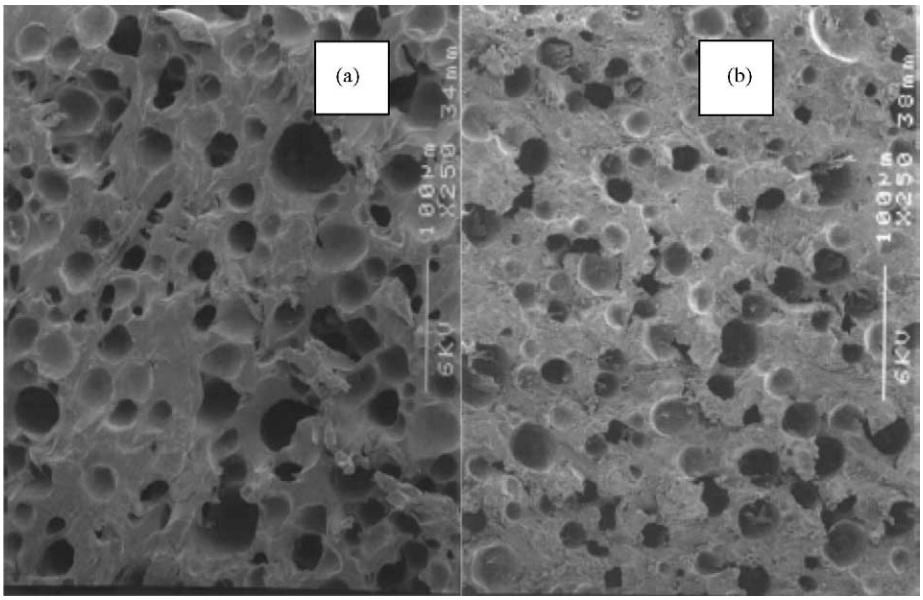

Fig. 66. (a) Scanning electron micrograph of CMP pad before and (b) after polishing [103].

It can be clearly seen that the pore size and shape distribution has been modified by polishing cycles. Polishing induced a permanent distortion in the radial direction due to the oscillatory motion of the wafer while no change was seen in pad pore size in the transverse direction (direction of pad motion). The change was attributed to pore closure by surface reflow of the polymer during polishing and conditioning and not due to debris filling [103]. Fig. 67a and b shows the pore distribution of the pad before and after polishing. The surface profiles generated using white light interferomery (WLI) by Lu et al. show that the overall micro roughness of the pad decreases with polishing and there is a smoothening effect over a period of time due to polishing cycles. Table 13 shows the value of roughness (R_a) in microns measured over the surface of the pad.

Along with physical changes, the pad undergoes surface chemical modification and degradation due to polishing slurry chemicals. The candidate pad used by Lu et al. was used for oxide polishing. When the new and used pads were evaluated for surface properties using XPS, the surface spectrum showed evidence of silica particles (abrasives) on the surface. Further analysis of Infra red spectrum of the silica film on the glass slide revealed that there is strong Si–O–Si stretching bond. Due to this the difference in the surface spectrum of new and used polishing pads cannot be completely attributed to

Table 13
Comparison of surface roughness before and after polishing [103]

Pad #1–14 location exp. times	R_a (μm)	
	New	Used
1	7.400	7.184
2	9.409	6.250
3	8.979	6.048
Average	8.596	6.494
S.D.	1.058	0.606

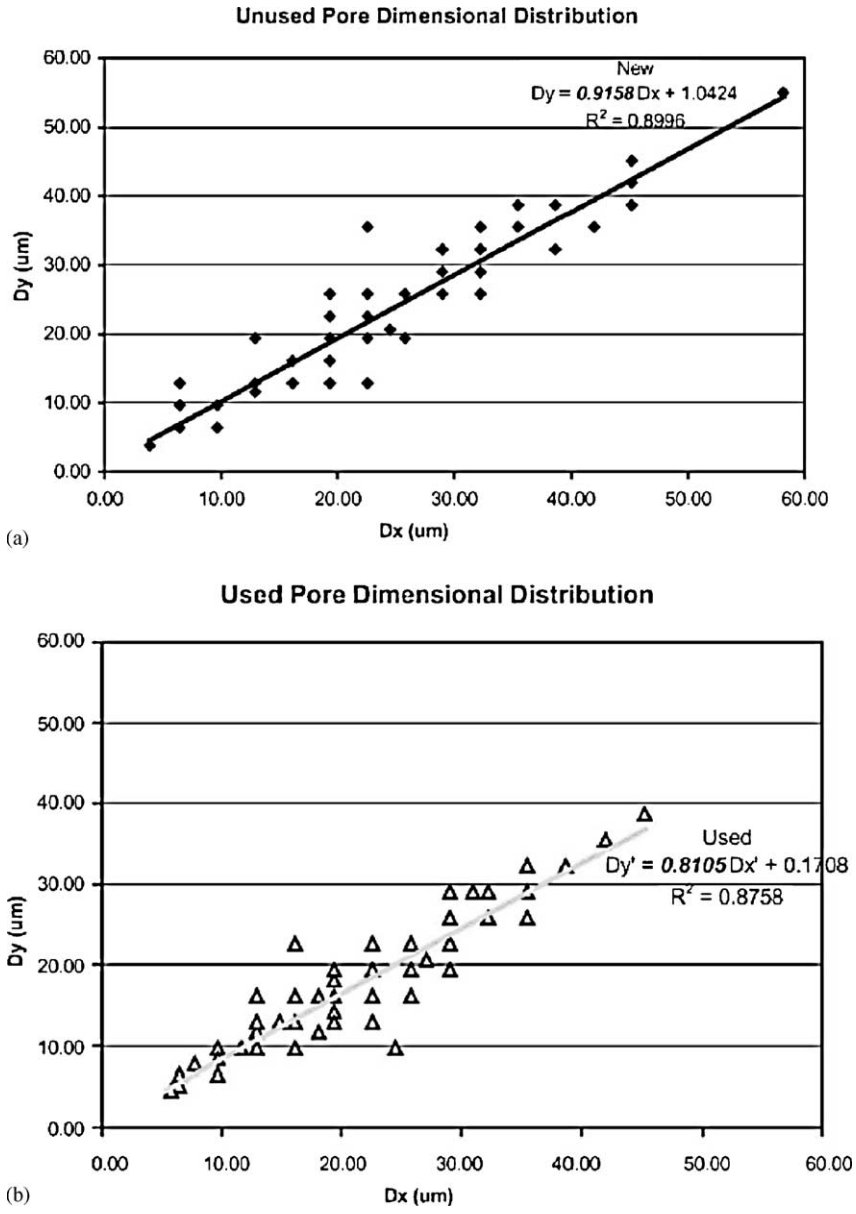

Fig. 67. (a) Pore distribution of unused; (b) used CMP polishing pad. D_x, D_y and $D_{x'}$, $D_{y'}$ correspond to the parallel and radial dimensions, respectively, in pores from new and used pad surfaces, where the slope of the linear relationship D_y/D_x is an indication of the degree of pore ellipticity [103].

the presence of silica debris. The absorbance spectra of new, used and dry silica slurry film (Fig. 68) evidently show that the change is surface is predominantly due to pad chemical degradation due to polishing and conditioning runs [103].

No pad degradation of the non-surface material of the used polishing pad was observed by Lu et al. indicating that the bulk material does not get directly affected by polishing. The change in spectrum and shifting of the peaks of used pad as compared to the new one has been attributed to the realignment of the molecules of the damaged pad surface layer.

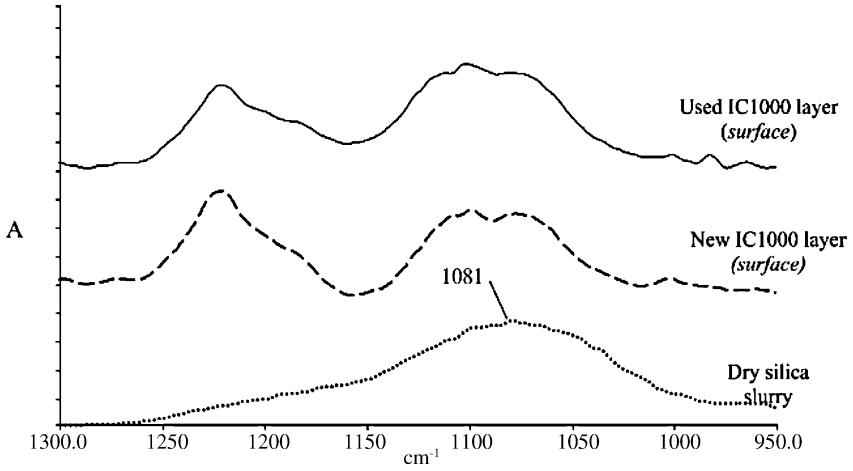

Fig. 68. The absorbance spectra in the 1300–1000 cm^{-1} region of used IC 1000 surface, new IC 1000 surface and dry silica slurry, respectively (from top to bottom) [103].

3.13. Effect of pad treatment

The porous structure of the polishing pad encourages water seepage. The presence of water in the polymer pore directly affects the mechanical properties of the polishing pad. Li et al. [171] studied the effect of pad soaking time on the mechanical properties of the polishing pad using DMA. Li et al. designed an experiment to progressively soak a pad in water and find the change in shear modulus (Fig. 69). The dynamic shear modulus decreased to two thirds of its original value when the pad is soaked for 5 h. Further, the rate of decrease in dynamic shear modulus dampens at around 14 h but does not reach a steady state. Li et al. [171] simultaneously performed and experiment to estimate the removal rate of the pad with soaking time in water. As seen from Fig. 69, there is no significant change in the removal rate when pads with different soaking time are used in oxide polishing. This shows that removal rate is more of a surface characteristic of the pad and does not get affected by the bulk material

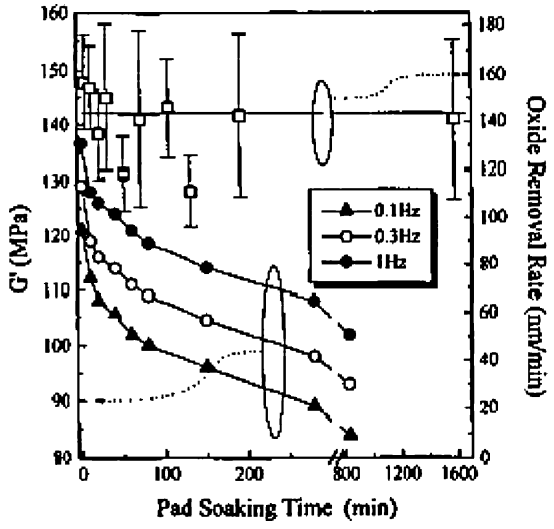

Fig. 69. Dynamic shear modulus (left) and oxide removal rate (right) vs. soaking time of an IC 1000 pad in water [105].

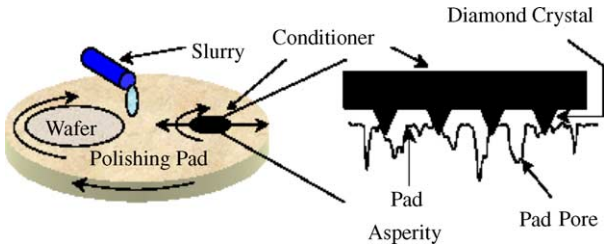

Fig. 70. Interaction between the pad and conditioner [186].

properties. However, the bulk material properties can directly impact other CMP parameters and hence need to be thoroughly evaluated.

3.14. *Effect of conditioning*

Modification of the pad wafer contact mechanics can directly impact the CMP process performance. The modified surface can even go up to changing the mechanism of material removal during a polishing process [182]. To quantify the change in the surface of the pad, Borucki [183] has proposed a probability density function (pdf) for time dependence of the variation in polishing rate due to the abrasive wear of the pad. Lawing has already shown that changes in the pad surface produce CMP results that deviate from the Preston's equation. Along with wafer polishing the conditioner made of diamond grit considerably alters the surface of the polishing pad. The interaction of the pad and conditioner can be seen in Fig. 70.

Fig. 70 shows the pad and conditioner surface geometry. The process of conditioning essentially removes some amount of top pad surface and is performed either in situ (during the polishing run) or ex situ in between two polishing runs. The pad damaged due to insufficient conditioned is termed as "glazed".

Experiments were performed by on CMP pad by Lawing at different conditioning aggressiveness (expressed as low, medium and high). The reduced polishing rate (i.e. polishing rate divided by the product of pressure and velocity of the condition corresponding to the polishing) was plotted as a function of predicted contact area and pad surface roughness. The change in polishing rate correlated better with the predicted surface contact area (details of predicting pad surface contact area have been published by Lawing [182]) rather than the surface roughness. The surface contact area is a pad near surface parameter, while pad roughness is a bulk parameter. Fig. 71 shows the variation of reduced polishing rate with pad surface contact area and pad roughness.

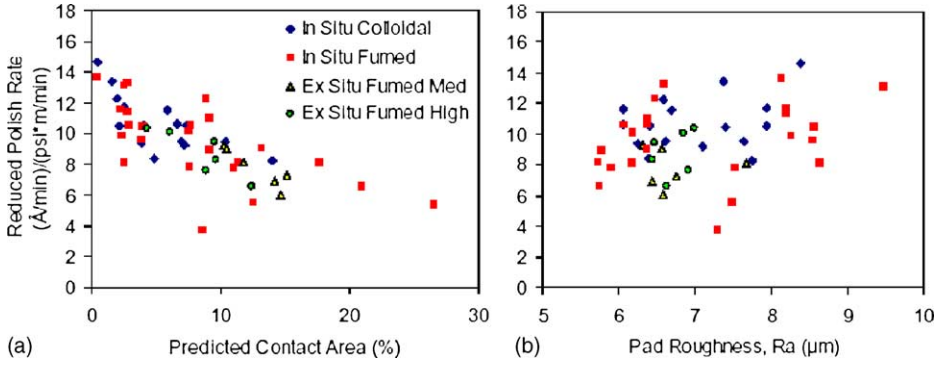

Fig. 71. Variation of reduced polishing rate with: (a) predicted contact area and (b) pad roughness [186].

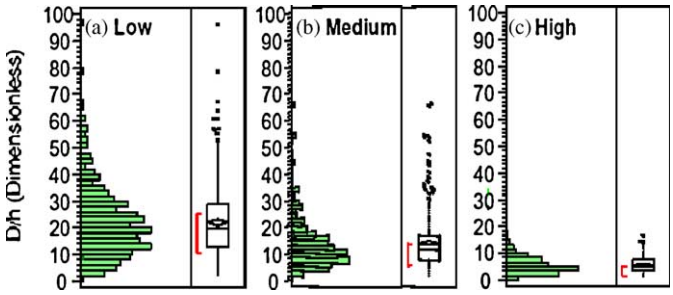

Fig. 72. Pad asperity distribution with different conditioning aggressiveness [186].

Fig. 72 shows the pad asperity distribution for different conditioning aggressiveness. The data represent pad surfaces after steady-state polishing utilizing in situ conditioning with conditioners of varying aggressiveness levels (low, medium and high pad dressing rate) and otherwise identical process conditions. It can be noted that the degree of pad surface deformation (relative area of red secondary peak) increases with decrease in pad conditioning aggressiveness.

3.15. Novel pads

Traditionally the Rodel IC 1000/Suba IV has been the pad of choice of semiconductor industry. However, the drop off in material removal rates as a function of time observed on polyurethane has been attributed to changes in the mechanical response of polishing pads under conditions of critical shear.

It has been shown before, that the functionality loss on polyurethane-based CMP pads is due to pad decomposition from the interaction between the pad and the slurries used in the polishing. Based on this understanding, we have developed and demonstrated a new class of application specific (ASP) polishing pad based on thermoplastic polyolefins. The application specificity is accomplished by matching the micro-mechanical properties of the pad surface to the material being removed during the CMP. The process advantages of the resultant ASP pads include: no need for the traditional pad 'break-in' before polish, no conditioning/dressing ever, no need to keep pads wet in idle mode, long pad life, high selectivity, ergonomically friendly/easy pad changes and demonstrated pad-to-pad reproducibility. The polishing performance and characteristics of the ASP have been elaborately discussed by Zantye et al. [173].

Currently the process of CMP is carried out using slurry with fine abrasive particles. This gives rise to a lot of practical difficulties in slurry handling. Slurry particle agglomeration a result of faulty handling and mixing and agglomerated particles give rise to lot of polishing defects such as non-uniformity and scratches. In order to over come these difficulties, embedding the abrasives in to the polishing pad has altered the conventional polishng method and this technique is called slurry free polishing technique [184]. The slurry free technique shows two distinctive advantages: (1) simplicity in handling and (2) cleanliness. Promising results on the CMP process using fixed abrasive pad have been reported recently [185]. Fig. 73 shows SEM of a 3 M fixed abrasive pad. The pad used in polishing wafers with different pH solution depending upon the process removal rate and uniformity requirements. The polishing solutions can be improved by adding different oxidizing and complexing agents.

3.16. Summary

The research in CMP consumables has generated a lot of knowledge about the dependence of the CMP process over the several consumable micro scale, meso scale and macro scale consumable.

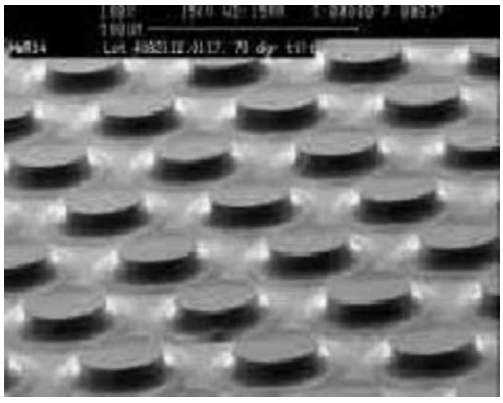

Fig. 73. Scanning electron micrograph of a fixed abrasive pad [188].

Influence of the slurry parameters on the CMP output variables has been discussed in the section. The dependence of the critical out put variables such as global planarization and removal rate has been emphasized. The parameters considered during the slurry design such as selectivity, particles dispersion, size distribution, etc. affect the CMP output parameters such as defects generation, removal rate, and planarity as well as the slurry polishing mechanism. Several defects that arise in CMP process due to faulty slurry characterization (microscratches, non-selectivity) have been discussed in this section. The polishing pad also equally influences the CMP process. The effect of pad mechanical properties on the CMP process and effect of different conditions and treatments on the pad mechanical properties themselves have been discussed. The polishing pad is conditioned to expose the new surface for polishing and even this has an effect on the CMP process. The polishing pad also causes several defects such as non-uniformity, dishing, erosion, etc. This section emphasizes that the properties of the pad when studied as whole can show variation even when different small samples of the pad appear to be homogenous. The physics and chemistry of the pad surface change before and after polishing have also been discussed. Finally new innovations in pad design and fabrication have been overviewed.

4. Chemical mechanical polishing of low-*k* materials

4.1. Introduction

Understanding the tribological, mechanical and structural properties of an inorganic and organic dielectric layer in the CMP process is critical for successful evaluation and implementation of these materials with the copper metallization. However, there are still many issues to be resolved, as integrating low-*k* is more complicated than the integration of Cu. Perfect dielectric materials should have high mechanical strength, good dimensional stability, high thermal stability, ease of pattern and etch for sub-micron features, low moisture absorption and permeation, good adhesion, low stress, good etch selectivity to metal, high thermal conductivity, high dielectric strength, low leakage current, good gap filling and planarization capability, and dielectric constant <3 [186–190]. Polishing behaviors of different carbon and fluorine doped silicon dioxide (SiO_2) low dielectric constant materials in chemical mechanical planarization process are discussed in this chapter. Tribological properties of SiLK and BCB dielectric films are also discussed here. Films were deposited using both chemical vapor deposition and spin-on method. Carbon and fluorine incorporation in the Si–O network weaken

Table 14
Properties of ideal low-k materials [184–186]

Electrical isotropic $k < 3$ @ 1 MHz	Chemical	Mechanical	Thermal
	No material change when exposed to acids, bases and strippers	Thickness uniformity <10% within and <5% wafer to wafer for 8 in. wafer at 3σ	$T_g > 400$ °C
Low dissipation	Etch rate and selectivity better than oxide	Good adhesion and good metal and other dielectrics	Coefficient of thermal expansion <50 ppm/°C
Low leakage current	<1% moisture absorption at 100% relative humidity	Residual stress < (±) 100 MPa	Low Thermal shrinkage
High charge trapping	Low solubility in H_2O	High hardness	<1 wt.% loss
High electric field strength	Low gas permeability	Low shrinkage	High thermal conductivity
High reliability	High purity	Crack resistance	
High dielectric breakdown voltage >2–3 M V/cm	No metal corrosion	Tensile modulus >1 GPa	
	Long shelf life	Elongation at break >5%	
	Low cost of ownership	Compatible at CMP	
	Commerically available		
	Environmentally safe		

the mechanical integrity of the structure and behave differently in slurry selective to SiO_2 films. Mechanical properties of the films were measured using depth sensing nanoindentation technique and found that undoped SiO_2 film has the highest and spin-on carbon doped oxide films has the lowest hardness and modulus values. Wear behavior of the doped SiO_2 is studied in a typical SiO_2 CMP environment and results are analyzed and compared with those of the undoped SiO_2 films. Coefficient of friction and acoustic emission signals have significant correlation with the polishing behavior. Surface of the films are investigated before and after polishing using atomic force microscopy (AFM). Roughness and section analysis of the films after polishing show the variation in wear mechanism. Validation of Preston's equation is discussed in this study. Polishing behavior of different other polymeric dielectric films have also been discussed here. Additionally, different wear mechanisms are presented and a two body abrasion model is proposed for the softer doped oxide films.

4.1.1. Materials selection criterion

As the feature size in integrated circuit is reducing interconnect technology requires new materials with desired set of properties. Choosing a new dielectric material is a big challenge with required electrical, thermal, and mechanical properties comparable to or better than those of SiO_2. There is no standard for next generation low-k materials. Ting et al. generated a list of required properties, shown in Table 14.

In summary, the important properties of the dielectric are essential [191]: (1) good thermal stability and low thermal expansion co-efficient are essential to prevent both damage to the film or property changes during thermal processes; (2) effective k values of the dielectric stack (dielectric, cap, barrier layers) should be less than 3.0; (3) good adhesion to withstand robust CMP process; (4) good etch and strip resistance. Potential for via poisoning comes from etching and resist removal. Etch processes have to be optimized for profile control and importantly, zero damage; (5) good mechanical strength to avoid delamination during CMP; (6) commercial availability and low cost of ownership.

4.1.2. Low-k present and future

The processing and integration of low-k materials creates challenges for the material properties and integration technologies. Several low-k materials are being discussed for integration with Cu in the future IC fabrication. It is necessary to consider an effective k value due to the presence of other dielectric layers in the stack. In the lower rows on the table, the predicted and effective k values are taken directly from the roadmap [192]. Among these materials, very few meet the thermal, mechanical, and electrical requirements for integrating them with metal. Low-k materials have to be mechanically strong enough, in order to resist delamination and mechanical breakdown during the CMP process. It can be seen from Fig. 74 that reducing the dielectric constant results in the degradation of the mechanical integrity of the materials [193]. In Fig. 74 the mechanical integrity scale hardness of different low-k materials was normalized with the hardness value of SiO_2. All low and ultra low-k materials are mechanically, chemically, thermally and electrically less stable than the historical material of choice, undoped SiO_2. Therefore, the challenge lies not only in identifying and characterizing the candidate materials, but also in devising the best methods to integrate those materials. As material dielectric constants get closer to 1, the materials become less robust and harder to integrate.

4.1.3. Overview of this chapter

Many researchers have proposed various low-κ materials, such as fluorine and carbon doped oxides, SiLK^{TM}, and other inorganic and organic materials as an alternative of SiO_2. Among them, fluorine and carbon doped oxides are very promising inter-level dielectric (ILD) materials, because of

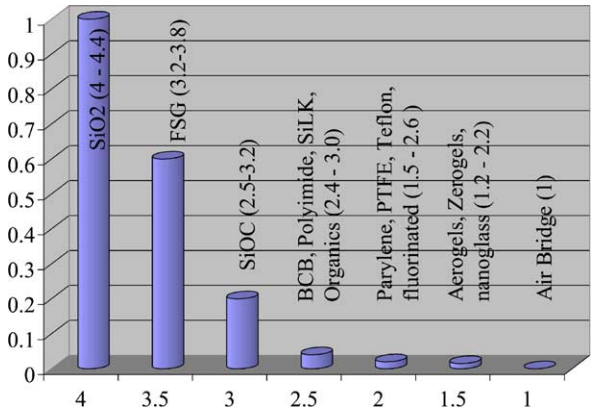

Fig. 74. Mechanical integrity scale of different dielectric materials normalized against SiO_2.

their high thermal and mechanical stability than that of organic materials [194]. In this study, we discussed the mechanical and tribological properties of different silicon dioxide-based interconnect dielectric materials (SiO_2, fluorine- and carbon-doped oxides). It is often difficult to study the fundamental polishing properties in situ in a real CMP polisher. Conventional studies mostly restricted themselves to the optimization of process parameters without understanding of basic tribological properties. The CMP tester (described in Section 2), used in this study, has several sensors (force sensor, acoustic emission (AE) sensor and electrical sensor), which are very useful for the in situ monitoring and optimizing the CMP process. Co-efficient of friction (COF) was measured using force sensor during polishing and it is found that COF has a dependency on hardness and acoustic emission. We have also discussed the correlation of AE signal with COF and mechanical properties of the films. Mechanical properties of the films were evaluated using nanoindentation while AFM technique was used to investigate the change of surface of the films due to polishing. Correlation of mechanical properties along with the friction behavior and surface nature of the films with the wear behavior has been discussed. Validity of Preston's equation has also been discussed. Different wear mechanism has been discussed and a two body abrasion model has been proposed for the softer films along with the normal CMP process.

4.2. Motivation for low-k CMP process understanding

In copper damascene process normally low-*k* materials are protected from exposure to CMP environment. It can be seen from Fig. 75 that low-*k* is ideally free from any polishing activity.

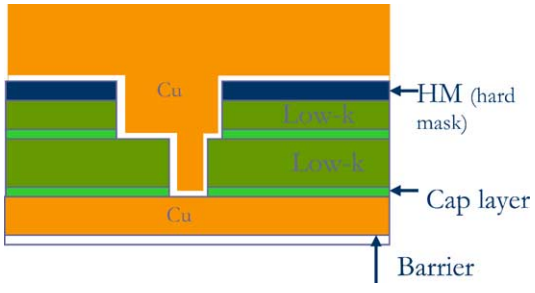

Fig. 75. Dual damascene structure.

In dual-damascene Cu-interconnect system CMP is a two step process. In first step Cu is being polished with a copper selective slurry and barrier layer, which acts as a protecting layer of low-*k* system. In second step barrier layer is being removed with barrier selective slurry and a hard inorganic mask/dielectric capping layer is typically used to provide mechanical support and prevent interaction between the slurry and the low-*k* materials. As the minimum feature size decreases barrier and hard-mask/cap layer dimension become critical in order to maintain the dielectric performance. Recent studies show that a copper interconnect system may indeed be feasible without barrier and hard-mask/cap layer [2]. Understanding of the tribological and corrosion behavior of low-*k* materials in CMP environment is due to: (i) evaluation of the scaling effect of copper interconnects technology with improving the knowledge on the slurry–dielectric interaction and (ii) development of new materials and CMP machine parameters suitable to eliminate the need for conventional barriers and low-*k* caps. In addition to these, the non-conformal deposition of spin-on polymers requires an effective planarization process. Preparation methods of next generation low-*k* materials may be restricted to only spin-on method. However, the planarization capability of the low-*k* materials has to be demonstrated prior to the implementation in these technologies.

4.3. Potential low-k materials

CVD and spin-on methods are main deposition techniques of present generation low-*k* materials. Several spin-on low-*k* materials, like hydrogen silsesquioxane (HSQ), spin-on-glass (SOG), SiLK (trade mark of Dow Chemical Company), etc. have been studied [195]. Low-*k* dielectric materials can be categorized as follows: doped oxides (FSG, HSQ, MSQ and HOSP), organics (BCB, SiLK, FLARE and PAE-2), highly fluorinated materials (paryleneAF4, a-CF and PTFE), and porous materials (aerogel and xerogel) [195]. In some cases, combinations of these materials (for example, porous organics) are also being explored [195]. Silicon dioxide (SiO_2) has a dielectric constant of $\sim$4, while air is considered as the perfect insulator with a dielectric constant of $\sim$1. Porous materials can therefore achieve lower dielectric constants than the constituent materials [196]. Among many low-*k* candidates, however, only a few materials have shown all the required properties needed for integration into high-volume manufacturing processes.

Finding polymers with low-*k* value is a relatively easy task; but finding those with all the required chemical, mechanical, electrical and thermal properties for use in IC applications is more difficult. Proponents of CVD approaches, most notably carbon-doped siloxanes also known as organo-silicate glasses (OSGs) with *k* ranging below 2.5, claim the advantage of being able to reuse of existing tool sets and simpler integration due to the SiO_2-like structure of CVD siloxanes [197]. Alternatively, manufacturers of spin-on materials and spin-on equipments contend the better extendibility of future generations' low-*k* dielectrics, especially in the sub-2.5 range when porous low-*k* materials will likely be used. Today, porous versions of many low-*k* spin-on materials are available for testing, whereas porous CVD low-*k* materials have yet to be demonstrated [197].

Most spin-on materials are organic polymers, some are inorganic and some are blends of the two. Their *k* values vary significantly from each other, depending on the material. However, in general the values are below 3.0. The semiconductor industry first broached the subject of new dielectrics in 1998 with the 0.18-μm circuitry that is now standard in high-end semiconductor chips like the Pentium 4. At this production node, manufacturers found a relatively easy answer for low-*k* material in fluorinated silicate glass (FSG), a CVD material created by doping traditional SiO_2 with fluorine from silicon tetra fluoride during the deposition [195].

4.3.1. CVD-based low-k

Relative dielectric constant for conventional SiO_2 films is in the range of 3.9–4.6 at the frequency of 1 MHz. The values depend on the source materials and formation technique. Basically the dielectric constant is defined by the dielectric polarization, such as electronic polarization, ionic polarization and orientational polarization. Since the electronic polarization is basically defined by atomic radius, the molecular structure differences are essential. The dielectric constant is also increased by residual H–OH/or H–OH absorption, due to orientational polarization increment. One of the techniques to reduce the electronic polarization is to introduce an atom with a small atomic radius in the Si–O networks. Hydrogen (H), carbon (C) and fluorine (F) atoms are very effective for this purpose. The binding energy of Si–F bond (129.3 kcal/mol) is higher than that of Si–O bond (88.2 kcal/mol), Si–F bond is thermally more stable. Therefore fluorination of SiO_2 films has been one of the main methods examined to reduce the dielectric constant of SiO_2 films [198]. Incorporation of fluorine in Si–O network causes a reduction of dielectric constant as a result of fluorine being the most electronegative and least polarizable element in the periodic table [199]. Additionally, precursors for depositing SiOF films are readily available and are inexpensive.

Several companies are developing low-*k* CVD films using a variety of carbon-containing precursors. The resulting organosilicate glass (OSG) films are also called carbon-doped silicon oxides (SiOC). The organic groups in OSGs invariably take the form of tetravalent silicon with a wide range of alkyl and alkoxy substitutions. In these films, the silicon–oxygen network seen in glass is occasionally interrupted, in a more or less homogeneous fashion, by the presence of organic functional groups, typically methyl ($–CH_3$) groups. Additionally, hydride (–H) substitution at silicon can also be present in the network. The film's lower *k* results due to these changes to the SiO_2 network and the reduced density of the OSG film relative to SiO_2. In typical CVD low-*k* films, 10–25% of the silicon atoms are substituted with organic groups. In amorphous OSG structure, the ratio of Si and carbon atom is typically 4:1 [200].

4.3.2. Spin-on low-k

The spin on deposition technique is particularly suited when good local planarization and gap fill is required for inter-metal dielectric. Both inorganic and organic films can be deposited by spin on methods and final structure of the film could be amorphous or crystalline. The dielectric precursors are used in forma of ''sol''. The thin film coating is performed by dispensing a liquid precursor on the center of the substrate which is spun on a spinner. The rotation of the spinner causes uniform dispersion of the solution. The resultant thin film is hard baked or soft baked and then sintered at an elevated temperature (300–400 °C). The sintering process ensures final cross-linking of polymer chains and results in mechanically stable thin film. Amorphous dielectric materials such as spin on glasses are coated using this method. A combination of hydrolysis in which there is a transition from Si–OR to Si–R functional groups takes place in presence of moisture and condensation process in which Si–O–Si structure is formed with elimination of H_2O to form the spin deposited film. The viscosity of the films increases sharply after spinning there by helping the film to settle on the substrate. Subsequently the gel is dried by baking or curing step [200].

In order to further reduce the dielectric constant of the ILD, porous films are made using spin on technique. The formation of more or less rigid skeleton before water extraction is an important point for formation of high porosity materials. The porosity can be induced in the material during the sol gel process or can be formed by using sacrificial nanoparticles or porogens. The details of various techniques to fabricate low-*k* dielectrics and methods to induce porosity have been extensively discussed in literature.

4.3.3. Different low-k materials

Various oxide-based low-*k* materials were deposited using CVD as well as spin-on methods. Preparation technique and precursor gases for different types of doped and undoped oxides studied are briefly discussed in this section. Undoped silicon dioxide (SiO_2 U) films were deposited on 8 in. Si wafer using PECVD method in a six-station sequential deposition system. The precursor gases were silane (SiH_4), nitrous oxide (N_2O) and nitrogen (N_2) and the substrate temperature was maintained at 400 °C.

SiOF is a fluorine-doped silicon dioxide film. It was deposited using inductively-coupled high-density plasma chemical vapor deposition (HDP CVD) method with SiF_4, SiH_4, O_2 and Ar at 400 °C. Details of the deposition method have been discussed earlier [201]. SiOF films grown by HDP CVD method has been shown to result in a film that has excellent film quality and gap fill characteristics [201,202].

The dielectric film SiOC SP is a carbon-doped silicon dioxide, also known as carbon-doped siloxane, or organosilicate glass (OSG). This low-*k* film was grown on Si substrate using PECVD method at 400 °C in a six-station sequential deposition system. The precursor used in this process is a cyclic 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS). TMCTS is prepared through hydrolysis of methyldichlorosilane to firstly form a linear siloxane polymer that is end capped with trimethylsilyl groups.

$$(CH_3)Si(H)(Cl_2) + (CH_3)_3SiCl \rightarrow (CH_3)Si{-}O{-}[SiHCH_3{-}O]_n{-}Si(CH_3)_3$$

$$(CH_3)Si{-}O{-}[SiHCH_3{-}O]_n{-}Si(CH_3)_3 \rightarrow \text{TMCTS} + \text{other cyclic compounds}$$

Another carbon-doped low-*k* film (SiOC NSP) was deposited using a different and non-standard precursor tetramethylsilane gas, with N_2O and N_2 using PECVD method at 400 °C in a six-station sequential deposition system. It is similar to the film SiOC SP.

In order to investigate the difference in CVD deposited low-*k* with the spin-on low-*k* we have also used a carbon-doped oxide-based low-*k* (SiOC SO), deposited by spin-on method. SiOC SO is siloxane polymer-based material and is an organic and inorganic hybrid. As this dielectric film was deposited by a spin-on method, it has flowable and planarizing characteristics.

Silica aerogel/xerogel which is known as nanoporous silica, has numerous properties which suggest applications such as low dielectric constant ($1.1 < K < 2.5$) materials for inter-level dielectrics for the next generation. The advantages of these materials, in addition to the low dielectric constant, include high temperature stability, pores much smaller than microelectronic feature sizes, deposition using conventional spin-on and vapor deposition methods, and precursors similar to those currently used in the microelectronic industry. SiLK is a new polymer from the Dow Chemical Company which does not contain silicon. A valuable feature of SiLK is its high thermal stability. SiLK films are prepared by spin-coating of dissolved initial products in organic solvents and curing [203].

As the dielectric constant decreases the mechanical properties of the materials deteriorate. This is undesirable for interconnect materials. A material with optimized mechanical strength is very much required for successful chemical mechanical polishing of these interlayer dielectric materials. Thus to ensure a low-cost packaging solution for low-*k* devices, issues regarding mechanical properties must be understood and considered as carefully as electrical properties [204,205]. In the case of porous materials of dielectric constant ~2, porosity near 65% are utilized. These materials are so weak mechanically that they may not be robust enough for the CMP process. Simplified classification of the low-*k* materials can be seen in Fig. 76.

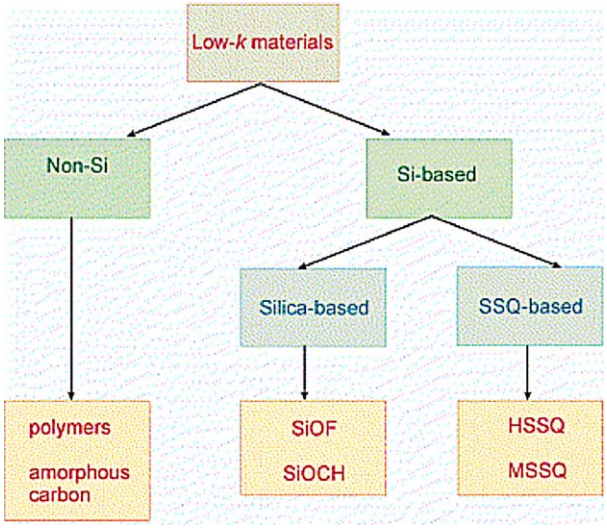

Fig. 76. Simplified classification of low-k dielectrics [205].

4.4. Mechanical characterization of low-k materials

To evaluate the mechanical properties, nano-indentation over a small scale has been used extensively in recent years [206–210]. This is a depth sensing indentation at low loads and is a well-established technique for the investigation of localized mechanical behavior of materials. The displacement and load resolution can be as low as 0.02 nm and 50 nN, respectively. A typical load versus displacement curve showing contact depth (h_c), and maximum depth (h_t) after unloading is shown in Fig. 77. Hardness and Young's modulus of elasticity are derived from the experimental indentation data by an analytical method using a number of simplifications [211]. Contact depth h_c can be calculated by:

$$h_c = h_t - \frac{\varepsilon F}{S} \tag{4.1}$$

where h_t is maximum depth of penetration including elastic deformation of the surface under load, F is the maximum force, and $\varepsilon = 0.75$ is a geometrical constant associated with the shape of the Berkovitch indenter [211]. Once h_c is determined, the projected area A of actual contact can be calculated from the

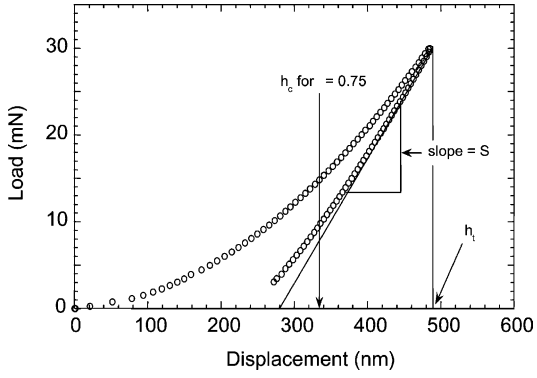

Fig. 77. Typical curve showing the loading and unloading as a function of indenter penetration depth.

Table 15
Details of different low-k materials [190]

Sample	Thickness (Å)	Grown by	Refractive index	Dielectric constant (k)	Film density
SiO_2 U	3850	PECVD	1.474	~4.0	~2.35
SiOF	1700	HDPCVD	1.430	~3.7	~2.07
SiOC SP	4350	PECVD and standard precursor	1.390	~2.9	~1.8
SiOC NSP	3550	PECVD and non Standard precursor	1.415	~2.9	~1.8
SiOC SO	6600	Spin-on	1.370	–	–

cross-sectional shape of the indenter along its length. S is the stiffness, which can be derived experimentally from the following equation:

$$S = \frac{dF}{dh} = \frac{2}{\sqrt{\pi}} E_r \sqrt{A} \tag{4.2}$$

where E_r is the reduced modulus. Hardness is then calculated from the simple relation:

$$H = \frac{F}{A} \tag{4.3}$$

The reduced modulus E_r is normally defined as:

$$\frac{1}{E_r} = \frac{1 - \nu^2}{E} + \frac{1 - \nu_i}{E_i} \tag{4.4}$$

where E and ν are Young's modulus and Poison's ratio for the sample and E_i and ν_i are the same for the indenter, respectively.

Details of the samples along with their refractive index, k-values, and density information are shown in Table 15. Mechanical properties of the films were measured using nanoindentation technique using Nano Indenter® XP (MTS System Corporation, Oak Ridge, TN). A three-sided Berkovich-shaped diamond indenter is used to indent on the material surface. The load and displacement data obtained in the nanoindentation tests were analyzed according to the method of Oliver and Pharr [206,207]. The continuous stiffness measurement (CSM) technique was used for measuring absolute and depth dependent hardness and modulus values. Values were calculated by averaging a number of separate indentations at particular depth specifications. Initially the instrument was calibrated with the standard sample (fused silica) provided by MTS and other single crystal metal samples.

Evaluation of mechanical properties of ILD materials is important because these coatings undergo multiple thermal cycles and CMP processes in IC fabrication. Additionally, mechanical properties of the low-k materials have been shown to depend on their k values. As the k value decrease the mechanical integrity of the materials deteriorate [193]. Depending on the mechanical properties of low-k films, consumables and machine parameters have to be selected during the CMP process. In this study, we have measured hardness and modulus of the thin blanket coatings of all doped and undoped oxide films using nanoindentation technique. Young's modulus and hardness for these samples are calculated from the loading and unloading curves using CSM technique and the results are summarized in Table 15.

One would expect though, that if the higher SiOF film thickness was available to measure the loading–unloading curve, results might not be very different than SiO_2 U film. This indicates that both the films might be behaving in similar way during the indentation. In other words, structural integrity

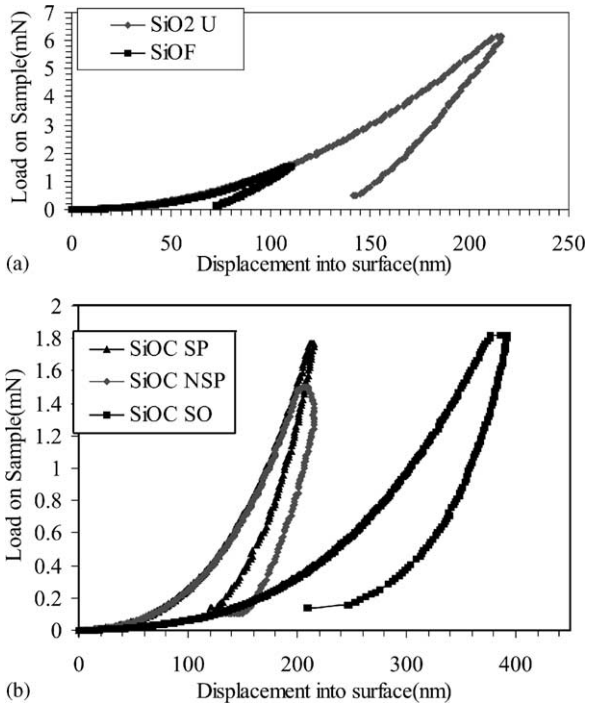

Fig. 78. Typical loading unloading curve for: (a) undoped SiO_2, SiOF and (b) SiOC (SP), SiOC (NSP), SiOC (SO) [212].

of both the films is not very different from each other. Also, both the films show more of an elastic nature during indentation process. Fig. 78b shows the loading–unloading curves for all three SiOC films. Although SiOC SP and SiOC NSP films show similar loading curve behavior, the unloading curve for SiOC NSP film shows more plastic deformation. Loading–unloading curve for SiOC SO film is very similar to that of a polymer-like soft material [212]. Before unloading, during hold time, the indenter displacement is taking place, which indicates that this spin-on film has time-dependent mechanical properties. The nature of unloading curve for SiOC SO film indicates the creep behavior of the film [213].

The modulus and hardness calculations were obtained from the plateau region of their respective curves versus penetration depth (∼10–15% of their film thickness range) in order to minimize substrate effects [214]. The results are summarized in Table 15. Although depth of indentation was set to 30–50% of the film thickness, absolute values were calculated at the average depth of ∼10% of the film thickness, which is a rule-of-thumb for measuring hardness and modulus of very thin films without substrate effects. It can be seen from Table 15 that SiO_2 U has the highest hardness and modulus values, whereas SiOC SO film have the lowest. Although the indentation behavior of SiO_2 U and SiOF films has similar characteristics within the measured depth of penetration for SiOF film, later has lower hardness and modulus. This is due to the incorporation of fluorine in the Si–O network which results in a feebler and less dense structure. It is prudent to mention that SiOF films with ∼10 at% of F in the structure exhibit film density of ∼2.07, whereas density of SiO_2 U films is ∼2.2–2.5 [194]. The modulus and hardness of SiOC films are smaller even when compared to that of the SiOF film. This again may be caused by the weaker mechanical integrity of the film, due to lower density of the films with carbon incorporation in Si–O network. The density of a typical SiOC film with carbon concentration of more than 10 at.% is ∼1.8 [194]. SiOC SP film deposited with standard precursor TMCTS exhibits lower hardness but higher modulus than that of the film SiOC NSP deposited with

Table 16
Details of the nanoindentation results

Sample	Thickness (nm)	Indentation depth (nm)	Hardness (GPa)	Modulus (GPa)
SiO_2 U	385	200	6.3 ± 1.2	68.1 ± 1.2
SiOF	170	100	4.3 ± 0.70	42.4 ± 3.4
SiOC SP	435	200	1.3 ± 0.17	8.8 ± 0.3
SiOC NSP	355	200	1.7 ± 0.50	6.1 ± 1.26
SiOC SO	660	350	0.3 ± 0.04	4.5 ± 0.5

non-standard precursor tetramethylsilane. It can be seen that uncertainty in the measurement of hardness and modulus are higher for the film SiOC NSP. Because SiOC NSP film grown with non-standard precursors may not be as homogeneous as SiOC SP film. Variation of mechanical properties of SiOC SP and SiOC NSP films are nearly similar. Very poor mechanical properties are obtained for the SiOC SO film. This is may be due to the fact that this spin-on film is a siloxane polymer-based material and is an organic and inorganic hybrid. The loading–unloading curves of the films also show the soft polymer-like nature of the films. The depth dependent hardness and modulus of all three SiOC films are shown in Table 16. It can be seen from Fig. 78 that the substrate effect on the mechanical properties of the SiOC SO films is lower with the indenter displacement than the others. This can be explained by plastic deformation of the film. Even a small change in k values has a remarkable effect on the mechanical properties of the low-k films [215]. As the k value decreases due to the reduced mechanical integrity, delamination is a major issue during CMP of Cu damascene process using low-k as interlayer dielectric materials (Table 16).

In another study, we performed nano-indentation on porous silica (xerogel) and SiLK low-k samples. Thicknesses were ∼600 nm, and the films were deposited directly on silicon using spin coating followed by thermal curing. The permittivity of these films were ∼2.2 (xerogel) and ∼2.7 (SiLK). High resolution scanning electron microscopy (HRSEM) is also employed in order to investigate the indent behavior on the film surface. Nano-indentation along with surface characterization is shown to be useful tools to investigate the mechanical behavior of low-k and other thin films.

Indentations on xerogel samples were performed at various depths ranging from ∼10 to 15% of the film thickness to more than the coating thickness in order to see the mechanical behavior of this low-k material. Typical loading–unloading curves versus displacement while changing penetration depth are shown in Fig. 79 It is seen from the figure that the loading and unloading curves for the xerogel samples are nearly the same. This kind of reversibility suggests that deformation due to indentation on the xerogel sample may be near elastic [211]. It can also be seen from the figure that all the loading curves for different indentation depths are following the same path, which indicates the reproducibility and uniformity of the coatings. The insert shows the curve at the lower indentation depth.

Loading and unloading curves at different depths of indentation on SiLK samples were performed and it was noted that the curves are less reversible than in the xerogel sample. This may be an indication of more plastic deformation during the loading. The inset shows the load–unload curve for low indentation depth.

The elastic modulus is the elastic response of the sample to an applied load and is equivalent to the stiffness of the sample. Young's modulus and hardness for the xerogel and SiLK samples are calculated from the loading and unloading curves using CSM technique and the results are summarized in Table 17. The modulus and hardness calculations were performed using the plateau region of their respective curves versus penetration depth (∼10–15% of the film thickness range). This minimizes the substrate effects [214].

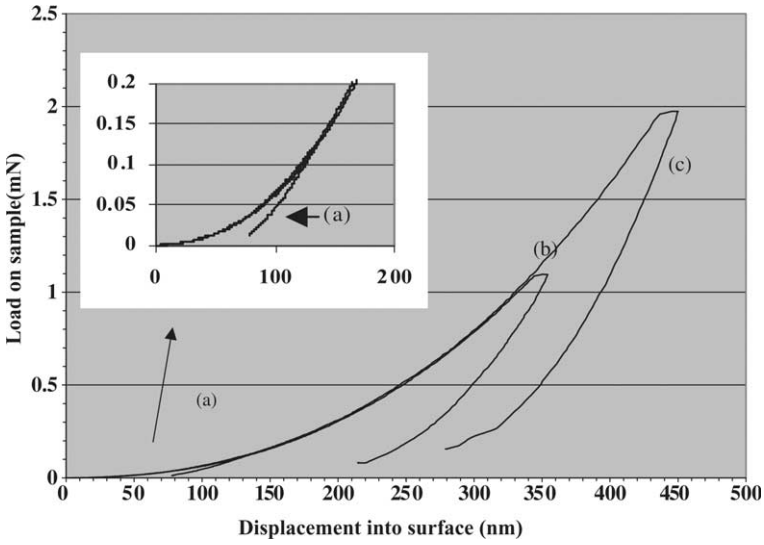

Fig. 79. Loading and unloading curves vs. penetration depth in xerogel sample: for h_t = 130 nm (a); h_t = 350 nm (b); and h_t = 450 nm (c) [212].

Indentation sites on the xerogel and SiLK samples were observed by HRSEM. Fig. 80 shows the micrographs of indented areas of both samples. Fig. 80a shows the indentation marks for a penetration depth of 2050 nm (∼3× the film thickness). The center of one of these indentations is enlarged in Fig. 80b. It can be seen from the micrographs that the xerogel coating is quite brittle and has been crushed or peeled from the substrate. Indentation marks for the 250 and 450 nm depths are also shown in Fig. 80c and d, respectively. It can be seen that radial cracks are being generated in both the 250 and 450 nm indents, but circular cracks are only visible after the 450 nm deep indentation. Fig. 76e and f show the indentation marks on the SiLK sample for the 250 and 2050 nm depth, respectively. These images also give evidence of delamination of the SiLK film from the silicon substrate after indentation, suggesting large tensile stress in the film (and limited adhesion), consistent with a thermally cured spin coating. Delamination of the low-*k* materials during CMP could be prevented with well characterizing the mechanical properties of low-*k* materials. Also mechanical properties of low-*k* can be correlated with the CMP performance of these materials. In the next section we will discuss the polishing behavior of various low-*k* materials in different CMP environment.

4.5. CMP of low-k materials

We have performed CMP process on a prototype CMP tester (UMT series, CETR Inc., CA) with variety of process parameters. It is essentially a bench-top CMP machine with a number of signals monitored and analyzed in situ. The polishing of the samples to be tested was performed with a variety

Table 17
Values of indentation results for xerogel and SiLK sample

Sample	Thickness (Å)	Displacement (nm)	Hard ness (GPa)	Young's modulus (GPa)	Depth of calculation (nm)
Xerogel	6000	100	0.29 ± 0.05	2.64 ± 0.31	35–50
SiLK	6000	60	0.26 ± 0.02	4.06 ± 0.25	35–50

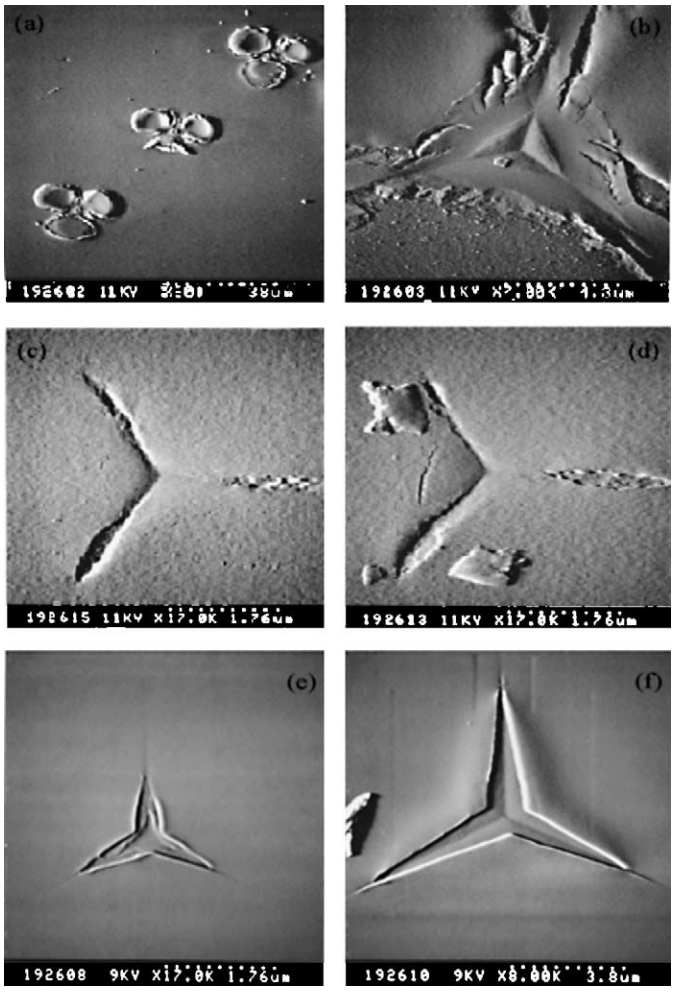

Fig. 80. SEM micrographs of indentation mark on the xerogel sample at different depth of penetration: (a) 2050 nm; (b) 2050 nm in higher magnification; (c) 250 nm; (d) 450 nm depth and on the SiLK sample at: (e) 250 nm; and (f) 2050 nm.

of process parameters after optimal settings of the machine were decided based on extensive experimentation. Details of the tester, its optimization and usefulness in studying CMP process have been discussed earlier [215,216]. CMP process conditions have been shown in Table 18.

Atomic force microscopy was employed to investigate the surface characteristics of the films before and after polishing. AFM experiment was performed on Digital Dimension 3100 instrument with silicon tip.

Table 18
Testing parameters and materials for measuring wear behavior of oxides

Normal pressure	Variable (1–6 psi)
Platen rotation	Variable (0.2–1.2 m/s or 42.2–254.6 rpm)
Slider movement	45 mm with offset ± 5 mm and velocity 10 mm/s
Slurry	Oxide slurry (Klebesol 1501) (100 ml/min)
Pad	IC 1000 B4/Suba IV
Time	20–80 s
Upper specimen	1 in. × 1 in. coupon of undoped and doped silicon dioxide

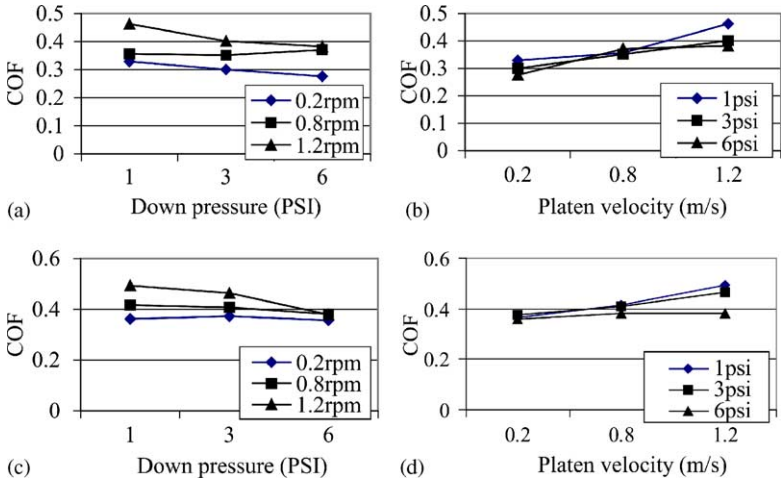

Fig. 81. (a and b) Variation of COF with down pressure (psi) and platen velocity (rpm) for SiO_2 U and (c and d) for SiOF films.

4.5.1. Doped and undoped oxide low-k materials

A series of doped and undoped oxide samples (1 in. × 1 in.) were tested at different combinations of down force and platen speed, while the slider was oscillating in the radial direction with a linear velocity of 10 mm/s and a radial distance 45 ± 5 mm. COF (coefficient of friction) is an important tribological property of the interface of films and pad, and was recorded during all the tests. Fig. 81a–d shows the COF versus psi and rpm during polishing of SiO_2 U and SiOF films, respectively.

Variation of COF with rpm and psi for the three different SiOC films is shown in Fig. 82. COF was calculated by taking average of 10–20 s data during the polishing of a total time of 20–80 s depending on the samples. A slight increase of COF could be seen with increasing rpm for both SiO_2 U and SiOF films. Additionally, the COF increases slightly for different psi for both the films. Values of COF are slightly higher for the SiOF films. It could be seen from Figs. 81 and 82 that variations of COF with rpm and psi for both SiOC SP and SiOC NSP film are similar to that of undoped oxide and fluorine-doped oxide films. It is interesting to see that COF for SiOC SO films does not vary much with both the variation of rpm and psi. Carbon-doped oxide low-*k* produces more friction than SiO_2 U and SiOF film. Difference in the variation of the COF for all the films may be caused by the dissimilar interaction of the Klebosol 1501 slurry selectivity to undoped oxide film and different surface nature.

In situ monitoring of the acoustic emission (AE) signal is performed in order to investigate the polishing behavior of different low-*k* materials. Every prototype material has a distinctive AE in a particular polishing environment. AE signal is also a measure of the intensity of polishing and this signal could be used for assessing the endpoint and defects of a particular polishing process. During polishing, the AE signal was monitored with time for all the polishing experiments and signal was averaged for a polishing time of 10–20 s. In order to compare the polishing behavior of the doped oxide films with the undoped films, AE values of all doped oxide sample are normalized with the values of undoped film.

The normalized AE values of all the samples at different psi and rpm are shown in Fig. 83. It can be seen that AE signal is nearly similar for both SiO_2 U and SiOF film, whereas the signal decreases for SiOC films. With few exceptions, AE signals are varying with the order of $AE_{SiO2\ U} > AE_{SiOF} > AE_{SiOC\ SP} > AE_{SiOC\ NSP} > AE_{SiOC\ SO}$. It is interesting to note that there is a correlation between mechanical properties of the films, described in the earlier sections, with the AE signals. Higher hardness and modulus values of the films result in higher AE signals. Fig. 83a and b shows that in

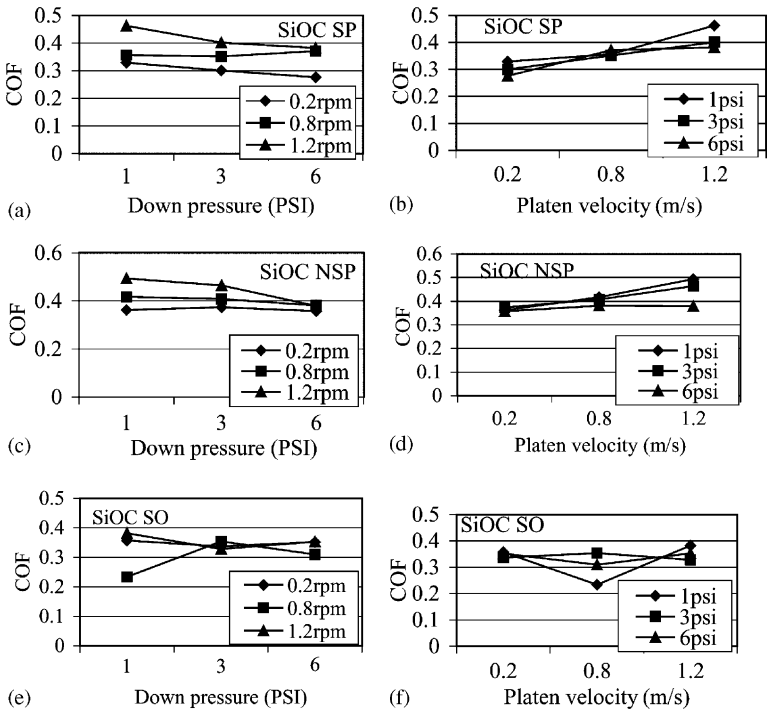

Fig. 82. Variation of COF with down pressure (psi) and platen velocity (rpm) for (a and b) SiOC SP (c and d) SiOC NSP and (e and f) SiOC SO.

general (except for SiOF film) AE values are increasing for higher platen velocity when polishing was performed at 1 and 3 psi. Exceptional behavior of SiOF film is not clear at this stage. Fig. 79c shows that polishing at 6 psi will result in an increase in AE signal as the platen speed is increased to 0.8 m/s. However, the AE signal decreased when the platen speed is increased to 1.2 m/s. Acoustic emission is used to measure the intensity of polishing, or in other words, to measure the interaction between the wafer surface, slurry and polishing pad. If the lower AE signal at higher rpm at 6 psi is due to hydroplaning, the effect should have been more pronounced at lower psi, which is not the case. A possible reason for the lower AE signal may be due to the reduced amount of slurry reaching in the interface of pad and wafer at this higher psi and platen velocity. This may also indicate the lowering of the polishing rate at these higher rpm and psi, and will be discussed more in details in the following sections.

4.5.1.1. Validation of Preston's equation. The material removal rate to validate Preston's equation was measured as described in Section 2. It is seen that removal rate increases with both rpm and psi for all the samples. It is seen that removal rate decreases slightly at platen rotation 250 rpm for SiO_2 U. If this is caused by inadequate slurry-film interactions during higher platen rotation, similar effect would have been seen for SiOF films also, and may be caused by hydroplaning effect at higher rotation. Validity of Preston's equation as described in Section 2 has also been tested for these different dielectrics and the results are shown in Fig. 84a and b which show the average RR versus rpm × psi for two types of films. The linear relation between RR and rpm × psi indicates that polishing of these films follows Preston's equation [99]. It can be seen that the data are more scattered for U-SiO_2 films than SiOF films. This may be caused by the higher mechanical polishing for SiOF films than chemical polishing, and uncertainty in the nine-point thickness measurements after polishing using

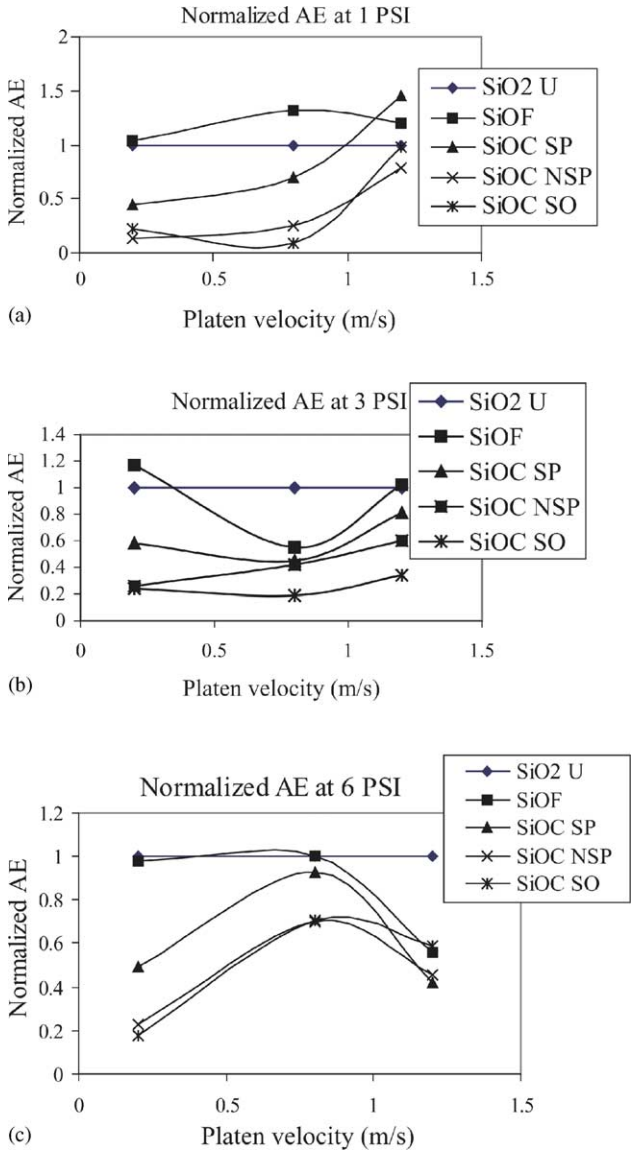

Fig. 83. Normalized AE signal of different samples during polishing at: (a) 1 psi; (b) 3 psi; and (c) 6 psi with varying platen velocity (rpm). Values of all the doped oxide samples are normalized with the values of undoped sample.

ellipsometer. It is assumed that the fluorine concentration does not bring a significant change to the oxide structure. Since the hardness of SiOF is comparable to that of SiO_2 U, it is safe to say that the polishing behavior of both the materials is similar. Validation of Preston's equation for all the SiOC films is shown in Fig. 85. Only SiOC SP follows Preston's equation. A very different behavior is observed in SiOC NSP and SO samples. SiOC NSP and SiOC SO (Fig. 85b and c, respectively) do not obey the Preston's equation, thus indicating that the polishing mechanism is different from a typical CMP process. The reason behind this aberration could be the dissimilarity in the chemical structures of the SiOC films deposited by different methods. It can be inferred that films deposited by standard precursor, SiOC SP are more suitable for polishing with typical oxide slurries, compared to SiOC NSP and SiOC SO films. Polymeric SiOC SO film shows little change with the variation of psi × rpm.

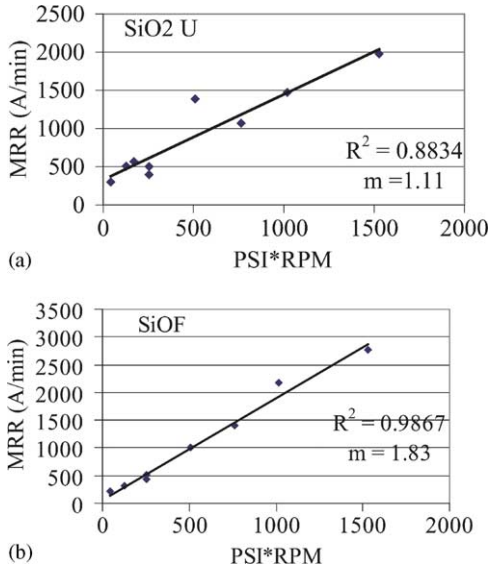

Fig. 84. Validation of Preston's equation for: (a) SiO_2 U and (b) SiOF films.

For SiOC SO films little variation of COF (seen in earlier section) and materials removal rate with the variation of rpm and psi indicate close relation of COF with the materials removal in CMP process. During polishing, it was observed that the carbon-doped samples were hydrophobic in nature when compared to the hydrophilic nature of SiO_2 U and SiOF films. The hydrophobic nature of the carbon-doped oxides was observed to be in the following descending order; SiOC SO > SiOC NSP > SiOC SP. To investigate the hydrophilic or hydrophobic nature of these films, a detailed study of their chemical nature is required. Pressure and velocity do not have the expected influence on all these samples. SiOC SO behaves like polymer materials as the chemical interaction between the slurry and the film may be different than that of the other oxide [217].

It can be noticed from Figs. 84 and 85 that SiO_2 U, SiOF and SiOC SP follow the Preston's equation with the slope (m, values shown in the figure) of the curve increasing as we go from SiO_2 U to SiOC SP. MRR is also increasing in the same order. Rate of increase of MRR is higher as psi × rpm increases for SiOC SP samples. Additionally, higher MRR rate is seen for SiOC NSP sample, although the variation with psi × rpm is less. MRR for SiOC SO is comparable with all the films, but much lower than the expected value as they are the softest films studied. From nanoindentation studies, it can be seen that SiO_2 U has the highest mechanical integrity, while SiOC SO has the lowest (Table 16). As expected, MRR is lower for SiO_2 U film. However, rate of increase of RR for other films is much lower than the rate of decrease of mechanical integrity. The RR of softer films should be much higher during mechanical polishing, which might not be true for chemical mechanical polishing process. This observation may indicate that when we consider the chemical polishing occurring in CMP, it may not follow the typical mechanical polishing behavior, suggesting that the material removal by the slurry on reaction with the wafer surface is not only dependent on the hardness of the film, but its reactivity with the surface of the films as well.

4.5.1.2. AFM surface investigation. To investigate the surface of the films after polishing and their influence on the polishing mechanism, some films were scanned before and after CMP using AFM. Films were scanned with an area of 1 μm × 1 μm and surface average roughness (R_a), RMS roughness

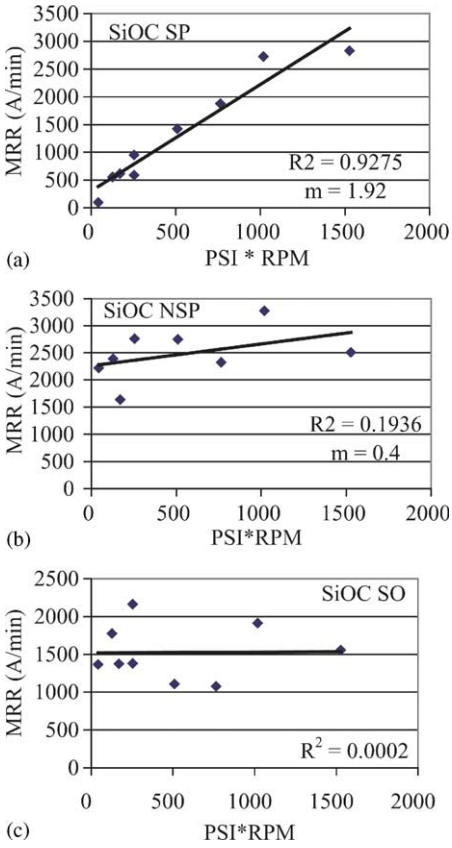

Fig. 85. Validation of Preston's equation in the material removal of three different SiOC films: (a) SiOC SP; (b) SiOC NSP; and (c) SiOC SO.

(R_{RMS}) and maximum heights (section analysis) were calculated. AFM results are summarized in Table 19. Surface view of unpolished and one of the polished samples (3 psi, 0.8 m/s) are shown in Fig. 86. It can be seen from Fig. 86 that PECVD SiO_2 U has highest surface topography with very high R_a (2.69 nm) compared to other doped oxide films. SiOF film possesses a very smooth pre-CMP surface (R_a = 0.14 nm), which may be caused by the smaller thickness of the film (170 nm). Among all the SiOC films, SiOC SP has highest pre-CMP roughness (R_a = 0.6 nm), while SiOC SO possesses lowest R_a (0.45 nm). Section analysis on the pre-CMP sample surface shows similar trend as surface roughness. It can be seen that post-CMP surface of all the different films polished at 3 psi and 0.8 m/s, shown in Fig. 86, possess smooth surface with material removal track on the surface. Circular material removal track on the surface may be due to the lack of upper sample rotation in the bench-top polisher used in this study. Roughness and section analysis on this post-CMP surface reveal very interesting insight of the polishing behavior, which may be characteristic of their materials properties. Post-CMP R_a value of SiO_2 U polished at 3 psi and 0.8 m/s is 0.28 nm with maximum feature 1.51 nm, while those of SiOF film are 0.27 nm (R_a) and 1.80 nm, respectively. It should be noticed that the pre-CMP roughness values of SiOF film were lower than that of the post-CMP film. Increased roughness and maximum height for the SiOF film may being due to the limit of polishing performance could be achieved by the pad and slurry used in this study. Similar roughness values for SiOF and SiO_2 U films are observed and may be due to the similar nature of materials removal with this set of CMP

Table 19
Summary of AFM results for the unpolished and polished at 3 psi with three different rpm

Sample (psi)	Platen velocity (m/s)	Average roughness (R_a) (nm)	RMS roughness (R_{RMS}) (nm)	Section analysis, vertical distance (nm)
SiO_2 U				
0	0	2.69	3.42	17.50
3	0.2	0.42	0.55	2.04
3	0.8	0.28	0.37	1.51
3	1.2	0.22	0.28	1.28
SiOF				
0	0	0.14	0.18	0.95
3	0.2	0.30	0.39	2.06
3	0.8	0.27	0.40	1.80
3	1.2	0.24	0.31	1.48
SiOC SP				
0	0	0.60	0.78	3.73
3	0.2	0.42	0.54	2.81
3	0.8	0.35	0.44	2.88
3	1.2	0.33	0.42	1.99
SiOC NSP				
0	0	0.54	0.68	3.48
3	0.2	0.34	0.43	2.77
3	0.8	0.42	0.53	2.50
3	1.2	0.295	0.372	1.935
SiOC SO				
0	0	0.451	0.557	2.665
3	0.2	0.483	0.612	3.634
3	0.8	0.624	0.793	4.335
3	1.2	0.335	0.416	2.342

consumables. Roughness and maximum height are higher for the SiOC films suggesting that the mechanism of polishing that is taking place on these soft films is different. Roughness and maximum height has increased remarkably for the SiOC SO film, whose mechanical integrity is the lowest among the three SiOC films. Removal of materials for SiOC SO films may be mostly due to higher mechanical shear. It is seen in the earlier section that MRR for SiOC SO does not follow Preston's equation. SiOC SP follows the Preston's equation in MRR while SiOC NSP follows Preston's equation a little better than SiOC SO film. AFM results along with the irregular MRR results for the SiOC SO strongly suggest the different mechanism of MRR.

Another interesting feature could be seen in surface finish after polishing at different platen velocity. The variation of R_{RMS} and maximum height (vertical distance) with different platen velocity at 3 psi down pressure were plotted in Fig. 87a and b, respectively. Most of the films show lower roughness and maximum height at higher platen velocity. For film SiOC SO, values increase until the platen velocity reaches to 0.8 m/s and then decrease. It is also seen from Fig. 87 that SiO_2 U possesses highest degree of planarity (lowest roughness and maximum height) and planarization decreases with the decrease of the mechanical integrity of the films. Lower roughness and maximum height at higher platen velocity may be due to lower and uniform pad deformation and uniform film–pad contact during polishing. This is also in agreement with the finite element modeling of pad deformation effect in CMP proposed by Bastawros et al. [218].

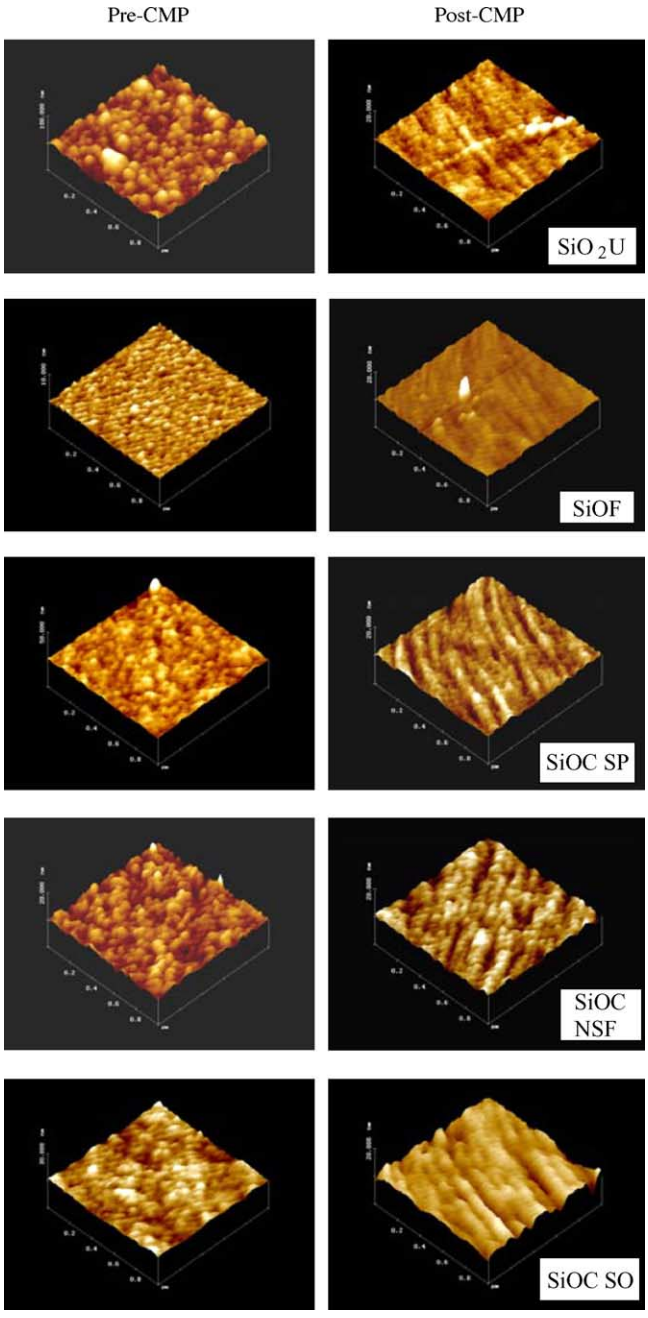

Fig. 86. Surface view of unpolished and polished low-*k* films. Polishing was performed at 3 psi and 0.8 m/s platen velocity.

4.5.1.3. Wear mechanism. All the films were polished with Klebosol 1501 slurry (pH 10.5) containing silica abrasives. In chemo-mechanical polishing, the reactivity of the slurry with the film surface is an important step in the complex materials removal process. Reactivity of the slurry with the film surface is highly dependent on the nature of the chemical bonding of the atoms in the film. SiO_2 CMP is one of the best understood CMP processes, since it has been studied for many years. It is widely

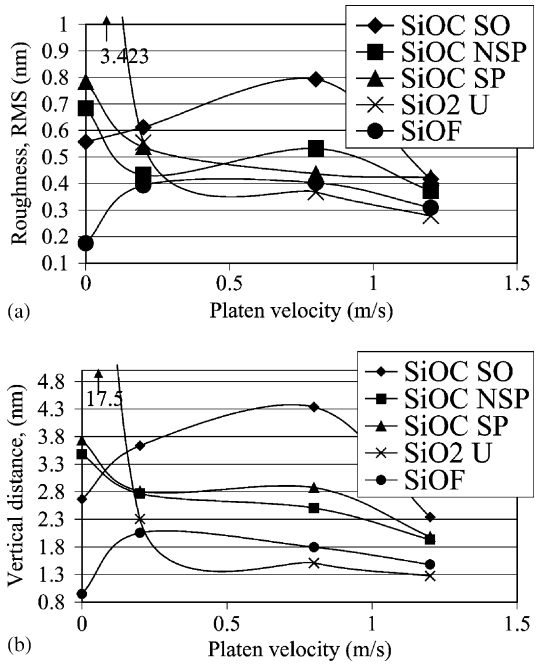

Fig. 87. Figures show the variation of RMS roughness (a) and vertical distance (b) with platen velocity.

believed that water diffuses into the oxide network and causes the rupturing of Si–O bonds [121]. Oxide surface weakening happens through the following equation: $\equiv$Si-O$-$Si$\equiv + H_2O \leftrightarrow \equiv$Si$-$OH. Once all of the Si–O bonds for a given Si atom are hydrated, $Si(OH)_4$ is formed which is highly soluble in water at high pH. The overall reaction is: $(SiO_2)_x + 2H_2O \leftrightarrow (SiO_2)_{x-1} + Si(OH)_4$. These reactions are accelerated by the compressive stress imposed into the surface by the abrasive particles. It has to be mention that Klebosol 1501 slurry has a silica abrasive which has equal hardness with the oxide surface and hence mechanical abrasion with the abrasive particles (particle indentation) will be negligible for oxide surface compared to softer film surface. In case of SiOF film, polishing with same oxide slurry leads to higher removal rate. Fluorine incorporation causes termination in the silica structure and less dense Si–O network, which leads to lower mechanical integrity [219,220] of the films. Reactivity of SiOF film with H_2O is higher due to the presence of defect sites such as non-bonding oxygen atoms and free volumes around Si–F bonding [221]. Si atoms linked with multiple F atoms have high reactivity with OH^- ions and H_2O [219]. Higher absorption of H_2O in SiOF network may also be enhanced due to the higher Si–O–Si bond angles in the SiOF films. Higher bond angle was confirmed by Kim et al. with observed blueshift in the Si–O stretching vibration model [194]. Removal of SiOF films with oxide-based slurry occurs similarly as removal of SiO_2 U film. Due to high water intake in the SiOF network and lower mechanical integrity of the film, the removal rate of this film increases accordingly. In this study, it was observed that although removal rate of SiOF is similar to that of SiO_2 U film at lower psi $\times$ rpm, this RR is much higher at higher psi $\times$ rpm (Fig. 84).

In order to investigate the material removal mechanism of PECVD SiOC film and spin-on SiOC film one has to consider the chemical change during polishing, the removal rate and surface roughness after polishing. SiOC dielectric family can be obtained by CVD or spin-on methods and they can be described as a hybrid between organic and inorganic polymer. In silicon oxide lattice, alkyl groups

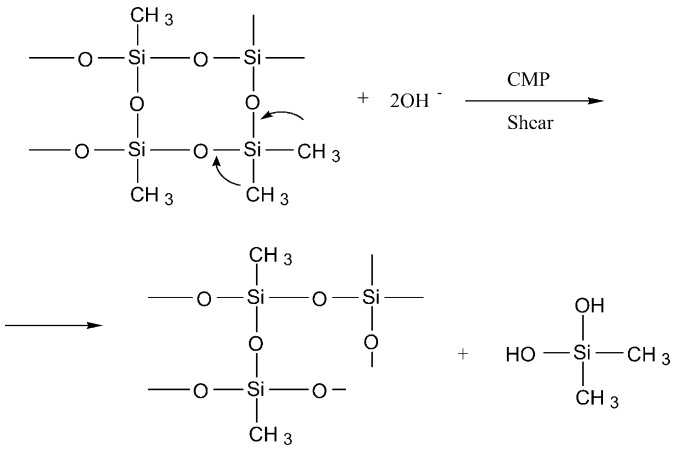

Fig. 88. Mechanism of materials removal of SiOC by slurry chemistry and shear.

such as $-CH_3$ could be bonded with Si, resulting in the introduction of carbon in the lattice. The carbon in the SiO_2 lattice leads to the formation of high-density nanopores (4–14 Å) [220], which causes the reduction of density, dielectric constant and mechanical integrity. Now investigating our experimental results on the SiOC films we first discuss the polishing mechanism of these films using the model suggested by Borst et al. [192] and then we propose a separate material removal model for the soft dielectric film. It is believed that oxide slurry and ambient water do not attack Si–C or C–H bonds, but attacks Si–O bonds, and material removal occurs through scission of Si–O structural bonds [192]. In this case, the materials are removed in groups of silicon which are attached with carbon groups, and the mechanism is shown in Fig. 88.

Among the three SiOC films, the SiOC SP follows Preston's equation, whereas SiOC NSP and SiOC SO do not follow. Also, all these SiOC films have higher removal rate than SiO_2 U film. It has been mentioned earlier that rate of increase of removal rate of these softer films is not equivalent to their decrease of mechanical integrity. Furthermore, SiOC SO is much more hydrophobic than SiOC SP. The AFM analysis shows that surface roughness is increasing as the mechanical integrity of the films decreases and the highest maximum height estimated in the SiOC SO film. Fig. 89 compares the maximum height of SiO_2 U and SiOC SO film after polishing. It is proposed in this study that in case of softer films, especially films of polymeric nature, material removal is more similar to a two-body abrasion. Luo and Dornfeld in their material removal model suggested that in solid–solid contact material removal is mainly due to two body and three body abrasion [123]. Materials removal by a abrasive particle attached with the pad is referred to as a two body abrasion whereas particles moving freely in the pad–wafer interface are involved in three body abrasion. Silica abrasives are much harder than these films and similar to SiO_2 U film. Penetration of these abrasive particles (acting as moving indenter) into the film surface will be higher in the softer films. In a solid–solid contact and assuming the abrasive particles of average diameter of the particle is r the depth of penetration of the abrasives into the film surface can be estimated from this expression. Penetration depth $z = 2F/\pi r H_f$, where F is the force applied on each particle and H_f is the hardness of the films [124]. Being in the denominator, hardness of the films inversely affects the material removal and surface roughness of the films. It can be seen from Fig. 89 that vertical distance in the film SiOC SO is much higher than that of SiO_2 U film, as the SiOC SO film has much lower hardness than that of SiO_2 U film. Material removal in this soft film is more like ploughing with a spherical indenter. Higher depth of grooves could be seen on the polished SiOC SO film (Fig. 89b) which is the softest film and polymeric in nature. Lower chemical

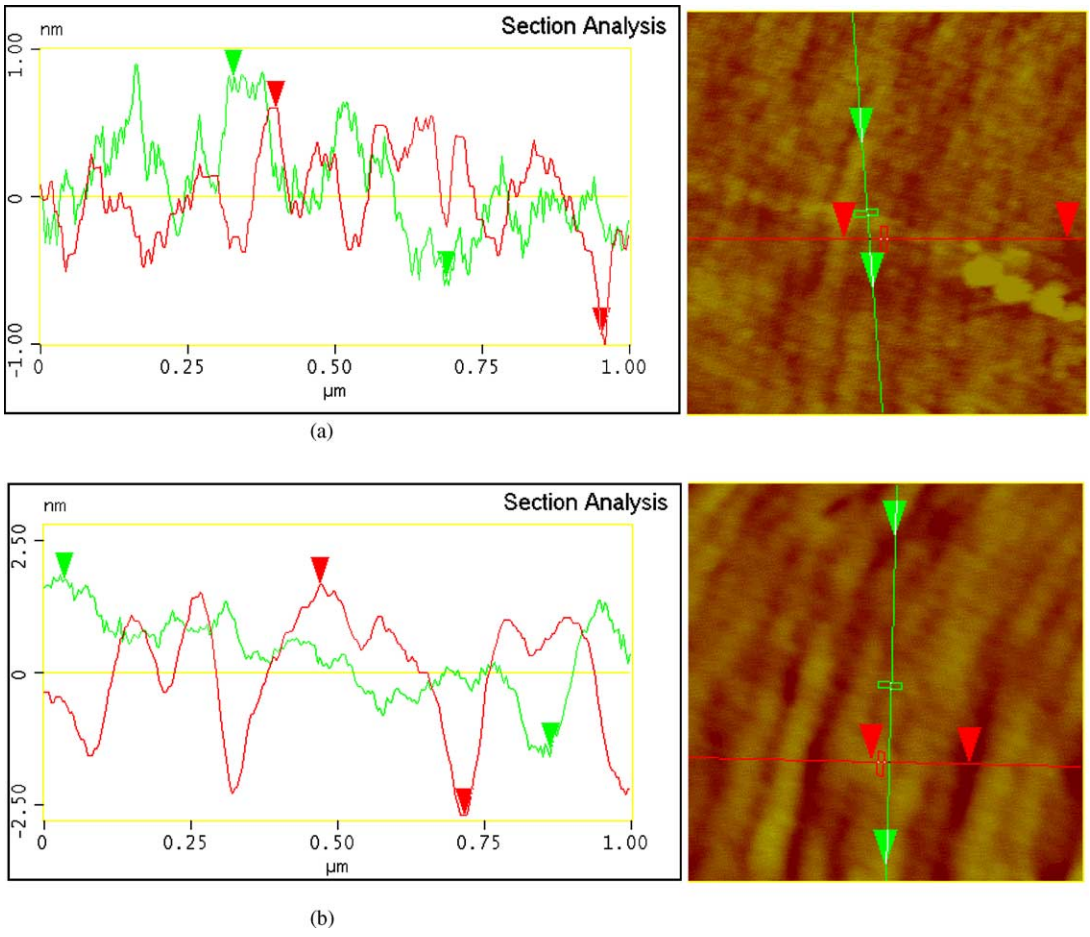

Fig. 89. AFM section analysis on the post-CMP surface of: (a) SiO_2 U and (b) SiOC SO films.

reactivity on this hydrophobic surface may be the reason for lower rate of increase of materials removal, although their mechanical integrity is much lower than that of SiO_2 U film.

4.5.2. Polymer material polishing

4.5.2.1. Polishing behavior of SiLK dielectric material. Hartmannsgruber et al. [217] studied the polishing behavior of blanket SiLK films using alumina-based slurry QCTT 1010 (RODEL) diluted with 30% H_2O_2 at a volume ratio of 3:1. CMP was carried out using a STEAG Mecapol E 460 polishing machine with a perforated IC 1000A/Suba IV stacked polishing pad (RODEL). The CMP parameters were a downward pressure of 22 kPa (3.2 psi), a backing pressure of 9 kPa (1.3 psi) and a platen and wafer rotation speed of 50 rpm. SiLK resin with a thickness of 1.8 μm was coated over Al test patterns having a height of 750 nm (Fig. 90). Their target thickness after polishing was 1.1 μm.

They investigated the planarization capability of the CMP process with evaluating surface topology of SiLK dielectric as a function of polishing time. The topography of the SiLK polymer caused by Al lines with widths of 0.5–400 μm before the CMP process is summarized in Table 22. A well-known definition to describe the achieved planarity after the planarization process is step height

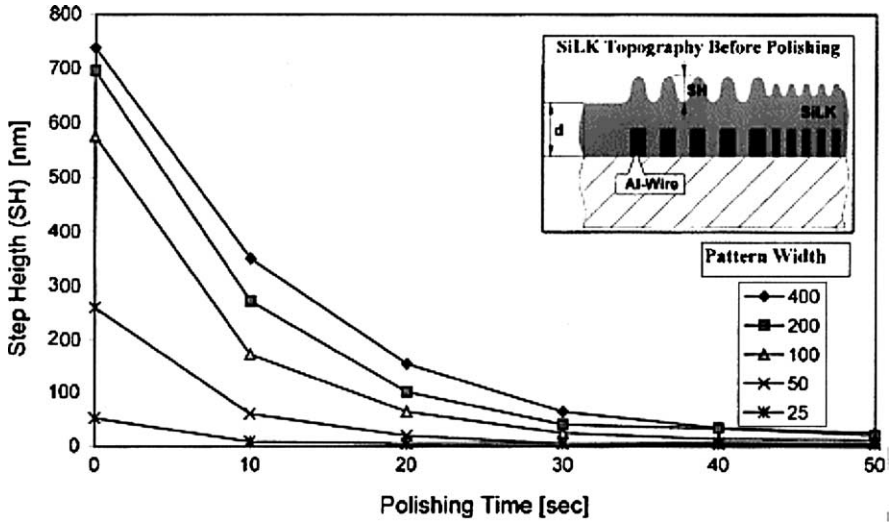

Fig. 90. Time and patterned dependent planarization of SiLK using the QCTT 1010 slurry [217].

reduction (SHR), which can be expressed by the following equation:

$$\mathrm{SHR} = \frac{\text{step height (SH)}_{[\text{before CMP}]} - \text{step height (SH)}_{[\text{after CMP}]}}{\text{step height (SH)}_{[\text{before CMP}]}} \tag{4.5}$$

The term step height reduction is normally only used after the complete polishing process. However, for the purpose of characterizing the polishing process itself, they have calculated the step height reduction after several intervals during polishing. The polishing time of each step was 10 s. The highest steps in the SiLK dielectric layer are caused by Al lines with a width of 400 μm (see Table 20). Step height reductions of more than 90% were achieved after only 40 s polishing time. The target thickness of 1.1 μm was achieved after a polishing time of 60 s and a SHR of more than 95% was measured. The higher values for SHR were measured, as expected, for the larger pattern, the higher topography of which was planarized faster than the lower steps caused by the smaller structures. The differences of the SHR between the chip located in the wafer center and edge are small and can be attributed to the process non-uniformity, which was not optimized for this study.

A comparative AFM investigation was made of the SiLK polymer surface before and after CMP. The AFM scans before CMP (Fig. 91) illustrate that the step height caused by five Al lines with a width of 1 μm is reduced from approximately 40 to <5 nm. The roughness of the SiLK coatings was determined at Al lines with a width of 6.25 μm after CMP and lead to post-CMP values of 1.1 nm (R_{ms}) and 4.0 nm (R_{max}) (Fig. 92). A slight increase of surface roughness was observed after polishing

Table 20
SiLK step height determined by profilometry [213]

	Profilometry					AFM		
Identical width and space between the line (μm)	400	200	100	50	25	6.25	1.00[a]	0.50[b]
SiLK step height (SH) (nm)	739	697	100	50	53	47	42	46

[a] The results of time and pattern dependent CMP planarization are summarized in Fig. 1. All features are planarized within less than 1 min.

[b] AFM measurement over five lines.

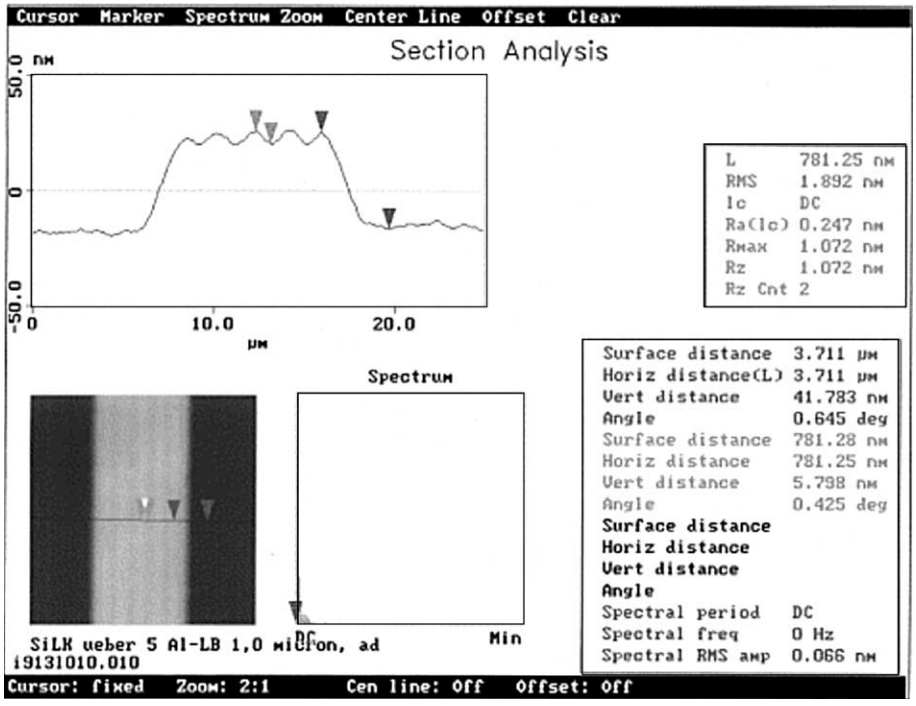

Fig. 91. AFM investigation of SiLK before CMP [217].

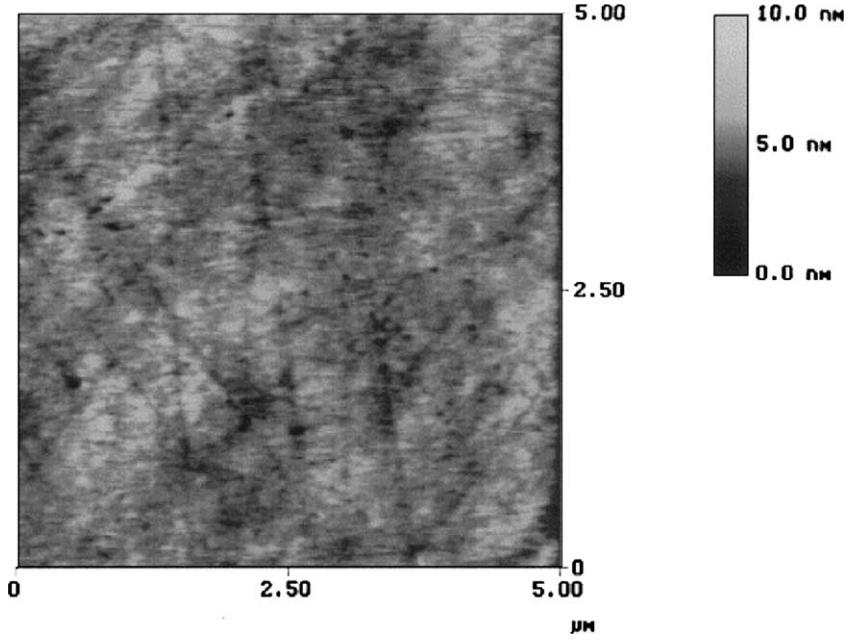

Fig. 92. AFM investigation of SiLK dielectric after CMP [217].

Table 21
Experimental details of slurries used for BCB polishing [188]

	Main components	Surface additive	Oxidizer	Abrasive (1.0 wt.%) Al_2O_3 (μm)
Control	DI H_2O_2 HNO_3 (1 vol.%)	None	None	0.05
Slurry 1	DI H_2O_2 HNO_3 (1 vol.%)	Triton-X 100 non-ionic (1 vol.%)	None	0.05
Slurry 2	DI H_2O_2 HNO_3 (1 vol.%)	Dow Fax 3BO amionic (1 vol.%)	None	0.05
Slurry 3	DI H_2O_2 HNO_3 QCT 1010	Unlisted commercial additive	H_2O_2 (3.3 vol.%)	0.05
Slurry 4	DI H_2O_2 HNO_3 QCT 1010	Unlisted commercial additive	H_2O_2 (3.3 vol.%)	0.30

Note: Control slurry is standard Cu slurry used to detect the effect of surfactants.

in the Cu slurry. Some micro-scratches with a depth of less than 10 nm caused by agglomerated Al_2O_3 particles in the slurry were detected. However, the level of micro-roughness is probably close to meeting the requirements of the subsequent process steps. A further reduction in surface defectivity is expected using improved slurry filtration methods. Their results illustrated the potential of this dielectric material for integration into existing Al/W-based interconnect technologies.

4.5.2.2. Polishing behavior of BCB dielectric material. To investigate the polishing behavior of the BCB polymeric materials, unpatterned samples of BCB 3022 and BCB 5021 were polished in different slurries as shown in Table 21 by Borst et al. [192]. Oligomeric solution (35 wt.%) was spin deposited and the cured at 250–300 in N_2 ambient. The BCB polymer was polished to study the output parameters such as (1) removal rate; (2) surface topography; and (3) post-CMP polymer surface chemistry.

Removal rate. Fig. 93 shows the variation of removal rate of the BCB samples in different slurries. The experiments were carried out at 2.5 psi down force, 30 rpm carrier, 30 rpm platen speed and 200 ml/min slurry flow by Borst et al. It can be seen from the diagram that the control slurry which does not have any surfactant does not show significant removal rate of the BCB while slurry 4 showed the highest removal rate. As BCB is basically hydrophobic in nature, there is latency in material removal. The low removal rate according to Borst et al. is also due to the lack of polymer weakening surface reaction of the slurry and formation of a passivation layer which protects the BCB surface.

Post-CMP surface topography. The results of atomic force microscopy studies performed by Borst et al. are shown in Table 22. There is an increase in the RMS surface roughness when BCB is

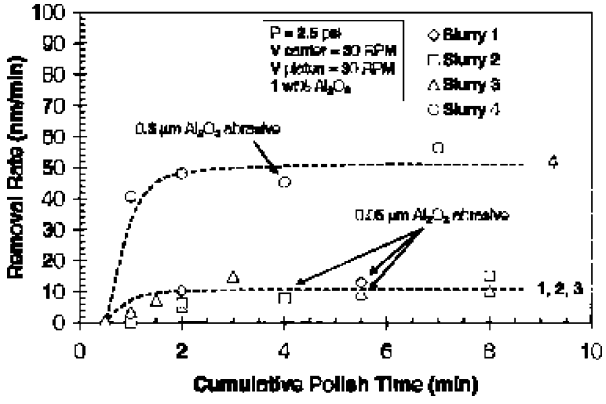

Fig. 93. The removal rate of Dow Chemical 3022 BCB in different slurries [192].

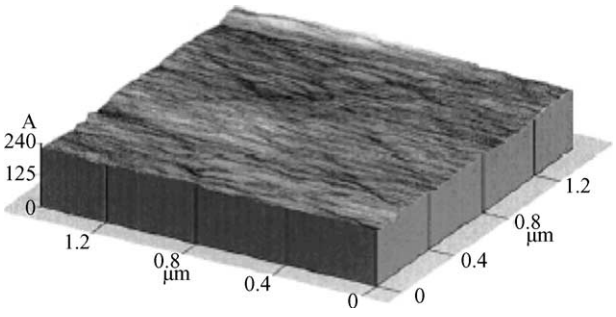

Fig. 94. Post-CMP AFM surface topography [2].

Table 22
Surface roughness data for BCB polishing [2]

	Time	Removal rate (nm/min)	RMS roughness (nm)	Comments
Unpolished	–	–	0.45	Smooth, as deposited
Control	8.0	∼0	Not measured	Extensive visible scratching
Slurry 1	5.5	10–15	1.4	Controlled abrasion after latency period
Slurry 2	8.0	10–15	0.7	Controlled abrasion after latency period
Slurry 3	8.0	10–15	0.5	Controlled abrasion after latency period
Slurry 4	7.0	45–55	1.3	Controlled abrasion after latency period

polished in all the candidate slurry. However, the values of surface roughness are different for different slurries. The added surfactant shows considerably reduced surface damage. The deposition of surfactant not only enhances slow and progressive material removal but also prevents significant materials damage. Fig. 94 shows the post-CMP surface topography of BCB.

Post-CMP BCB polymer surface chemistry. The post-CMP polymer surface chemistry evaluation was performed by Borst et al. using X ray photoelectron spectroscopy (XPS) as seen in Fig. 95a–c. The studies were performed using the angle resolved technique which probes 1–10 nm deep in the surface. Different angles gave the composition of bonding and various incident depths. Samples were measured after performing CMP with slurry 4. Table 23 shows the post-CMP altered surface layer atomic concentration. The post-CMP oxygen atomic percentage increased from 3 to 14 wt.%. The increase in atomic weight percentage was reflected in carbon peaks in form of –C–O and –C=O bonds. The constant oxygen content suggested that after sustained exposure to slurry, the oxidation reached equilibrium. The stabilization and hardening of the surface and resistance to scratches and damages during CMP was attributed to the oxidation of the surface.

Table 23
Post-CMP surface atomic concentration of BCB polymer studied by XPS [188]

Sample	Angle (°)	Depth (nm)	F (1s) (at.%)	O (1s) (at.%)	C (1s) (at.%)	Si (2p) (at.%)
BCB Unpol	90	10	–	3.5 (±2.2)	90.5 (±4.0)	6.0 (±0.4)
BCB	20	1–2	–	14.3 (±2.2)	80.8 (±4.0)	5.0 (±1.2)
BCB	45	5	–	14.3 (±2.2)	81.2 (±4.1)	4.5 (±0.2)
BCB	20	10	–	14.8 (±2.2)	80.6 (±2.0)	4.6 (±0.2)

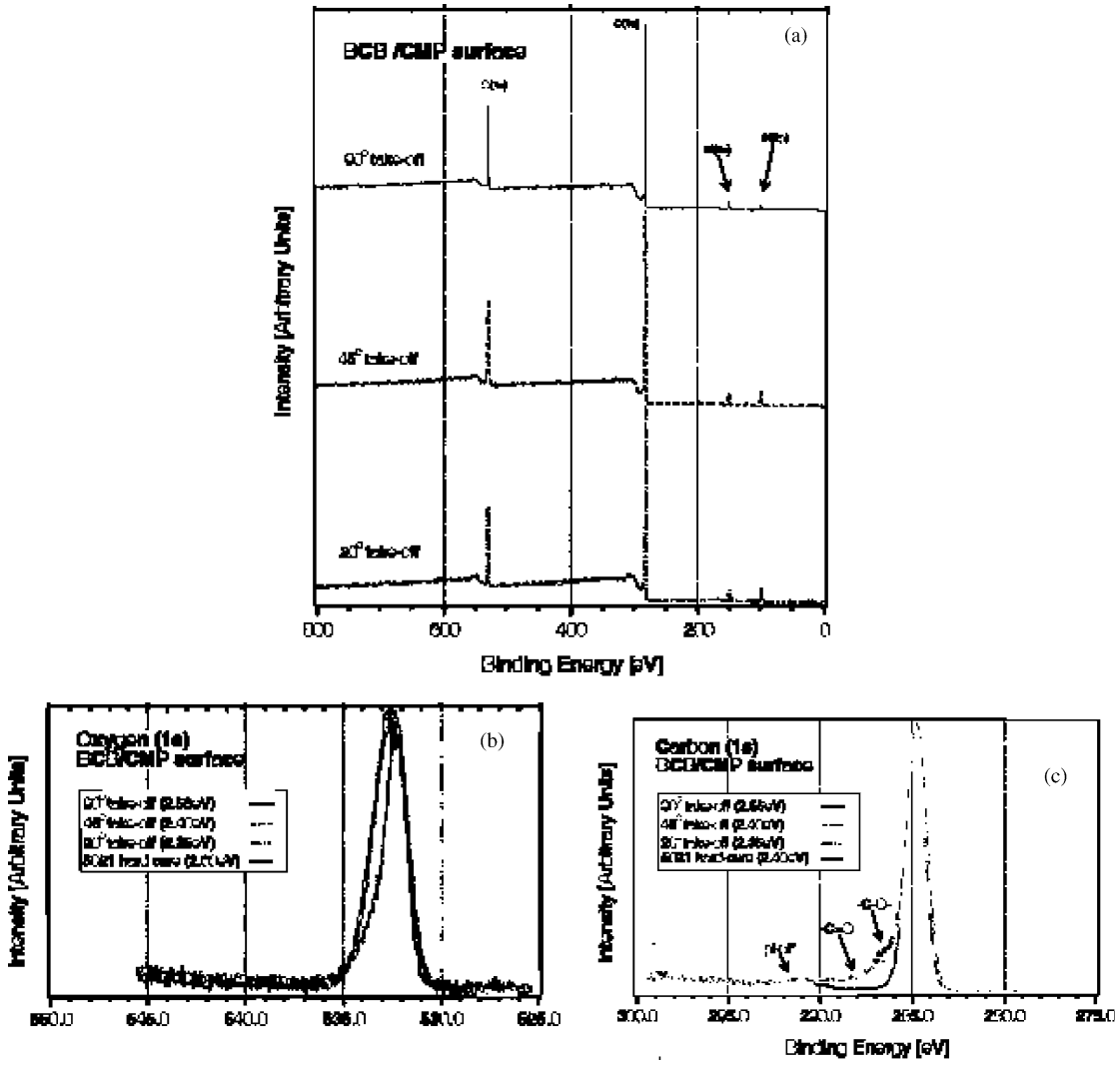

Fig. 95. (a) XPS spectra of BCB 5021 after CMP with slurry 4 for 10 min; (b) binding energy windows for oxygen (1 s); and (c) carbon (1 s) bonds show increased –C–O– and –C5O bonds at the BCB surface [222].

4.6. Modeling of polishing of dielectric materials

4.6.1. Oxides and doped oxide polishing

The mechanical interaction between wafer, pad and slurry has been the subject of research for sometime [222–226]. The most basic and most referred model to describe the CMP process was first given by Preston [99]. It states that the material removal rate (MRR) = K_pPV. According to Preston's equation the removal rate is directly proportional to the pressure (P) applied and the relative velocity (V) of the pad. K_p is the Preston's coefficient. In his equation, the pressure applied $P = L/A$, where L is the load applied and A is the area contacting the pad. This area of contact need not necessarily be the geometric area of the surface or the actual area of surface, because wafer surfaces (mostly patterned) have severe topography or a rough surface. In such a case, it cannot be assumed that the area on which the load acts is the geometric area of the surface being polished. Because of this reason many researchers opined that Preston's equation holds good only when there is a smooth surface. Preston's

equation has proved to be reasonably accurate for SiO_2, Cu and W (tungsten) CMP from the work reported by others. But the dependence of K_p on process variables like slurry composition and pad properties was not well understood.

Experimental results show that the slurry composed of abrasives and pad materials, has larger influence on material removal rate than just the platen speed and down pressure [226–229]. Several models that predict and explain the material removal mechanisms in CMP have been reported [99,226–231], most of which are based on the mechanical aspects of CMP. Some of the important aspects in addition to pressure and velocity are properties of consumables like the pad and slurry. Minute details of the pad: like the asperity distribution, asperity height and asperity radius also have shown to affect the rate of material removal [232]. Oliver [233] proposed an asperity contact model for CMP. Their results indicate that the polish rate is a sensitive function of the asperity height distribution. A modification to Preston's equation to account for the dependencies of removal rate on pressure and rotational speed during CMP process was made by Tseng and co-workers [219]. They proposed (MRR) = $MP^{5/6}V^{1/2}$, where M is the weighting factor to removal rate from other processes like slurry attack. Shi and Zhao [234] proposed another model that was contrary to Preston's model. Their experiments were carried out using a soft polishing pad. They proved with experimental results that pressure dependence of the removal rate for CMP with soft pads is non-linear. They also stated that there is a difference between polishing with a hard pad and a soft pad. Their model states that (MRR) = $K_{sz}P^{2/3}V$, where K_{sz} is a function of other CMP variables. In the case of soft pads, pad hardness is much less than the hardness of the abrasives and the wafer surface. Certain important factors are not considered in this model, for example, if the contact area increases there will be a decrease in the force applied on the abrasives, which will lead to smaller amounts of material removed by each. Shi and Zhao [234] recognized this limitation of the model and introduced a threshold pressure P_{th}, arguing that only when the down pressure is larger than the threshold pressure material removal will occur. They revised the earlier equation and proposed an equation to include the threshold pressure, which is given by MRR = $KV(P^{2/3} - P_{th}^{2/3})$, what is exactly included in the all-purpose coefficient K is still unclear [219]. Most of the models mentioned above do not take all possible scenarios into consideration. Some of them studied the behavior of pressure and velocity in contrast to Preston's equation. For example, Zhang and co-workers [235,236] proposed an equation MRR = $K_p(PV)^{1/2}$ taking into account the normal stress and shear stress acting on the contact area between abrasive particles and wafer surfaces.

However, most models were quite inadequate. Few researchers have considered only the pad effects while few others have considered only the effects of slurry flow. As the knowledge of CMP process and the role of consumables improved over the years, the material removal rate models also improved. Ahmadi and Xia [231] proposed a model for mechanical wear in CMP process by taking into account different possible cases. Basically mechanical contact theory was used to develop a model for pad asperities with abrasive particles in slurry and wafer. Different cases of pads (hard and soft), slurries (dilute and dense) were analyzed. In their work the material removal rate variation with pressure, abrasive size and concentration as well as pad characteristics (asperity distribution, pad elastic and plastic deformation) were studied. According to Ahmadi and Xia [231] the wear in CMP occurred in four different ways; abrasive wear, adhesive wear, corrosive wear and erosive wear. They believed that in CMP, abrasive and adhesive wear, are the main wear mechanisms. Their removal rate model stated that MRR = $s\mathrm{RR}_{\mathrm{abrasive}} + (1 + s)\mathrm{RR}_{\mathrm{adhesive}}$, where s is the probability that the abrasive particles will roll against the wafer during CMP. Their paper includes polish rate models for different cases like removal by abrasive wear and removal by adhesive wear, each of these cases having sub cases like abrasive wear with hard pad and dense slurry, abrasive wear with hard pad and dilute slurry, adhesive wear with soft pad and dense slurry and adhesive wear with hard pad and dense slurry with plastic deformation etc. But even here the chemical effects on CMP were not considered.

Apart from models that predict removal rate, a few models that control the CMP process by a run-by-run controller design were also proposed in literature [237]. Many models, some based on fluid dynamics, some on contact mechanics, some physics-based models, some chemistry-based models, some statistics-based models and some mathematical models were proposed by several researchers [238–243]. Most of the models worked on improving the Preston's equation as Preston's equation could not express exactly the effect of consumable properties on the removal rate. Also it could not be used for accurate removal rate prediction. A model proposed recently by Luo and Dornfeld [123] is the subject of investigation in this paper. This model was chosen in comparison to most other models existing in literature because it not only includes macro scale details of the process but also micro scales details associated with the consumables used. Their model is focused on studying the material removal occurring due to contact between the abrasive–pad and abrasive–wafer interfaces. Their model integrates process parameters including pressure and velocity in addition to other important input variables like pad and wafer hardness, pad roughness, abrasive size, abrasive size distribution and abrasive geometry and is given by the basic expression

$$\mathrm{MRR}_{\mathrm{mass}} = \rho_{\mathrm{w}} N \mathrm{Vol}_{\mathrm{removed}} + C_0 \tag{4.5a}$$

where the mass of material removed ($\mathrm{MRR}_{\mathrm{mass}}$) is equal to the amount of material removed ($\mathrm{Vol}_{\mathrm{removed}}$) by a single particle of the slurry in unit times the number of particles actively involved in material removal (N). ρ_{w} is the density of the wafer material and C_0 is the material removed due to chemical etching. The above stated equation gives a skeleton representation of the model. The detailed expression and explanation of the model with the assumptions and derivations are given in the coming sections of the paper. From the above discussion it is seen that the CMP process is a complex process because of the various factors that should be considered in order to characterize the process and achieve a globally usable model. Luo and Dornfeld proposed one such model in 2001 [125].

The three-dimensional fluid-mechanics and mass-transport CMP model developed by Sundararajan et al. [244] and Thakurta et al. [245,246] is the framework for solving complex multi step CMP reaction kinetics equations. Certain assumptions such as laminar flow, infinitely hard pad, no asperities, wafer thickness, etc. need to be made to elucidate the model output. Borst et al. [192] proposed that a CMP model for polymeric dielectric like SiLK in terms of five step surface mechanism that can be represented mathematically and solved using fluid mechanics and mass transport equation. The five steps of SiLK CMP can be listed as (1) mass transport of reactant from the bulk slurry to the slurry/wafer interface; (2) adsorption of reactant to available SiLK polymer surface sites; (3) reaction between adsorbed reactant and specific SiLK polymer surface sites to form an altered polymer surface layer; (4) shear-enhanced desorption of weakened altered polymer surface layer; and (5) mass transport of polymer product from the slurry wafer interface to the bulk slurry. Fig. 96 shows the multistep surface mechanism including the forward and reverse reaction, surface mechanism of forward and reverse reactions. Conservation of surface sites in this manner is crucial to representing the model using this modified L–H formulation. The mathematical formulation of the surface reaction, mass transport and slurry–surface interaction is elaborately discussed by Borst et al. [2]. Each of the equation is related to some boundary conditions and can be solved in groups by applying boundary conditions such as flux of the reactants. This information is used to calculate a flux of C_{R} to the wafer surface and C_{P} away from the wafer surface, which is related to the CMP removal rate

$$\mathrm{RR} = -\frac{1}{n}\frac{\mathrm{MW_P}}{\rho_{\mathrm{P}}} D_{\mathrm{R}} \frac{\partial C_{\mathrm{Ri}}}{\partial z} \tag{4.6}$$

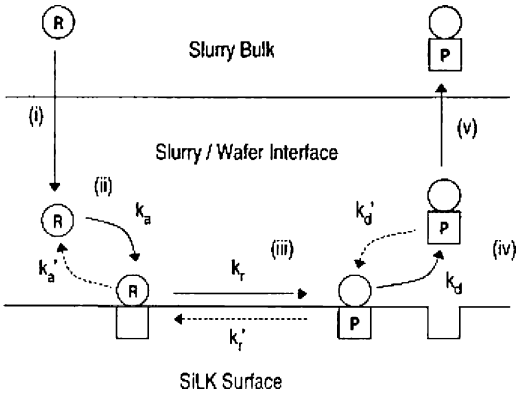

Fig. 96. Multistep surface mechanism [192].

where RR is the predicted SiLK removal rate, n is a stoichiometric constant equal to the number of reactant molecules and polymer reactive sites required to sufficiently weaken one section of the SiLK polymer structure, MW_P is the molecular weight of one altered section of the SiLK polymer structure (the product that desorbs from the wafer surface), ρ_P is the density of the altered polymer product, and D_R is the diffusivity of the reactant component in the slurry. The experimental results used to validate the model have been detailed by Borst et al. [192].

4.7. Defects in low-k materials

The deposition of conformal and uniform polymeric low dielectric constant films poses a challenge. There is also the ensuring that a defect free porous thin film gets deposited by methods such as spin on deposition and CVD. Furthermore, the challenges for low-k materials also include the CMP feasibility and integration in Cu damascene structure [245]. Fig. 97 shows the increase in porosity with decrease in dielectric constant.

The low dielectric constant materials that are integrated in the present day semiconductor industry are indicated in the shaded area [245].

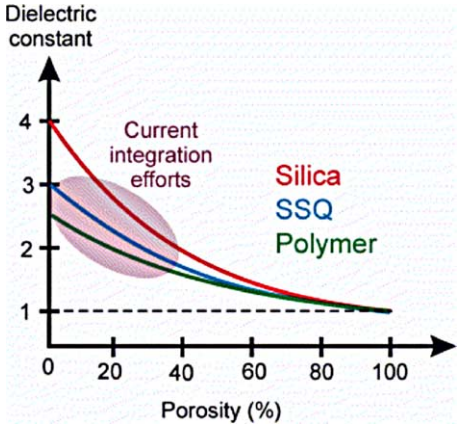

Fig. 97. Relative dielectric constant (k-value) as a function of porosity for different dielectrics [205].

The major low-*k* issues that have been elaborated by Shamiryan et al. [205], namely: (1) hydrophobicity, (2) mechanical stability, (3) thermal stability, (4) chemical stability and physical stability, (5) compatibility and (6) reliability have been discussed in this section.

4.7.1. Hydrophobicity

It is an absolute necessity for a low-*k* material to be hydrophobic. This is dues to the extremely polar nature of the O–H bonds. The dielectric constant of water is close to 80 and any presence of even small quantity of water that might be absorbed from the environment significantly tends to increase the *k* value of the materials. As water is abundant in air and even controlled environments have a humidity of 40–60%, it is a imperative that the low-*k* material is designed to prevent degradation in presence of such moisture content. Due to their large surface area per unit volume which could potentially encourage attack by water, porous materials needs to especially designed to withstand high moisture conent in the environment. Hydrophobicity is usually achieved by the introduction of Si–H or Si–CH_3 bonds. Oxygen-free organic polymers are generally hydrophobic.

4.7.2. Mechanical stability

There is a need for mechanical stability of the dielectric materials after introduction of Cu as the materials of choice for interconnect wiring. Previously, when Al was used in interconnects, the substrate was coated with Al, patterned using photolithography and Al wires were left behind unwanted. Al was removed using plasma etching. The dielectric was then deposited in space between the free standing wires. Unfortunately, Cu does not form valatile compounds with reactive gases and, therefore, plasma etching cannot be used. As a result, the damascene process is used to fabricate the present day interconnects. The substrate if first coated with dielectric, patterned, etched and trenches are formed where Cu must be present. A Cu seed layer is then deposited first by PVD and Cu is electroplated in to the trenches and the excess Cu is polished away. The technique has been discussed earlier in the paper and gets it name from the city of Damascus where swords were fabricated in this fashion. In order to achieve mirror like flat surface, the dielectric also needs to undergo, the mechanical stress of Cu removal and CMP. Low-*k* dielectric materials must also be able to survive stresses induced by the mismatch of thermal expansion coefficients or mechanical stresses during the packaging process, when fully processed circuits are connected to the outside world.

As has been shown earlier in this paper, the mechanical properties show a marked deterioration with increase in porosity. The Young's modulus of bulk SiO_2 decreases from 76 GPa to several GPa for materials with 50% porosity (Fig. 98). As the Young's modulus of low-*k* material drops below 10 GPa, integration becomes far more challenging (Fig. 99). Thus porosity of the low-*k* material needs to be maintained as low as possible with the simultaneous achievement of decrease in dielectric constant for a successful dielectric material. However, as the film porosity increases (Fig. 99), the Young's modulus drops with integration of the film becoming more difficult because of the mechanical instabilities associated with the decrease in Young's modulus and hardness. This gives rise to numerous modes of dielectric material failure such as cohesive failure and failure due to creep and delamination.

4.7.3. Thermal stability

The temperature that a die is subjected to during interconnect fabrication, packaging, soldering etc. is in the range of 400–450 °C. A low-*k* material must withstand the temperature that the entire die is subjected to. This is an impediment for some organic polymers as they begin to decompose at lower temperatures, implying severe restrictions on thermal processing and reducing the choice of polymers. In SSQ-based materials, elevated temperatures cause the conversion of SSQ cubes into silica tetrahedra, increasing the *k* value of the material.

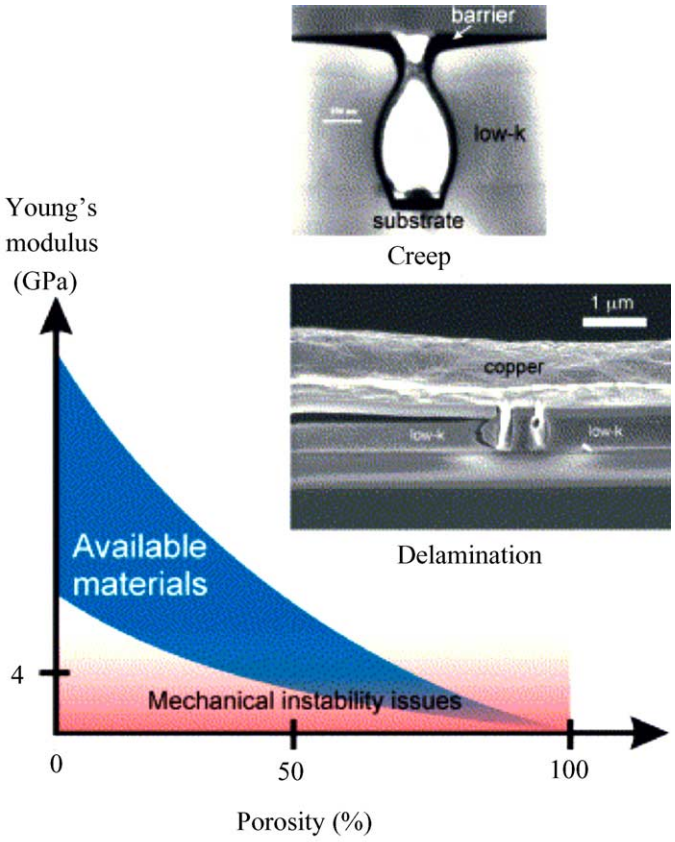

Fig. 98. Mechanical properties (Young's modulus) of low-*k* films as a function of porosity [205].

4.7.4. Chemical and physical stability

A low-*k* material must be able to withstand processing steps such as patterning and etching when trenched are made to fill Cu in to them. For example, oxygen plasma used during patterning (trench etching) or cleaning of low-*k* material can break Si–H, Si–C, and Si–CH_3 bonds, replacing them with Si–O. This increases the *k* value by introducing bonds of higher polarity and reduces hydrophobicity, which makes the material prone to water adsorption. In case of highly porous materials, this formation of Si–O bonds to increase *k* value along with the decrease in hydrophobicity can lead to particularly damaging effects. It should be noted, though, that these processes can be tuned to reduce their effect on low-*k* materials.

4.7.5. Compatibility with other materials

The compatibility of dielectric materials with other materials incorporated in the IC is a broader requirement which needs to be studied from different perspectives. The three major concerns could be highlighted, namely: (1) coefficient of thermal expansion (CTE), (2) barrier deposition, and (3) adhesion. A low-*k* material must be compatible with Cu in terms of CTE. This issue has to be especially taken care of when organic polymers are implemented as they have severe mismatched of CTE with Cu. A low-*k* film must also be compatible with the diffusion barrier, used to prevent the highly diffusive material Cu from entering the dielectric. Cu, otherwise shows a tendency to readily degrade the dielectric properties of the insulator and increasing the leakage currents there by significantly decreasing the breakdown voltage. As a result, the reliability of devices significantly

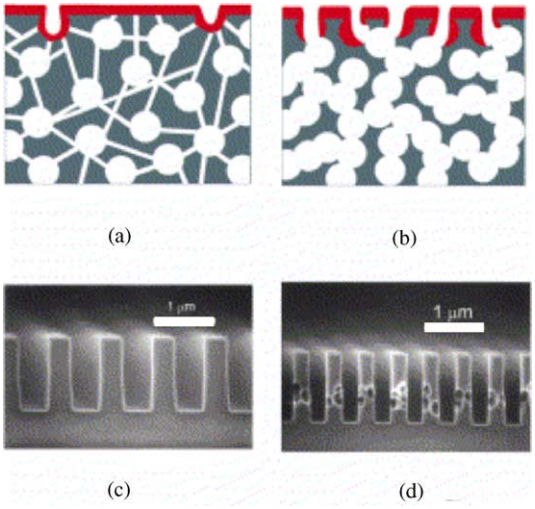

Fig. 99. A schematic representation of a thin film deposited on a porous material with: (a) separated mesopores connected by microchannels and (b) interconnected mesopores. As porosity increases, the mesopore connections make the deposition of a continuous film more difficult. The photos show examples of barrier integrity tests by HF dip. A fully continuous barrier (c) prevents HF from attacking the underlying dielectric, but discontinuities or 'pinholes' in the barrier allows HF to attack the dielectric (d) [205].

decreases, making their lifetimes unacceptably short. Cu diffusivity drastically increases with dielectric porosity. There is no allowable tolerance as far as the barrier stopping Cu diffusion is concerned. The barrier must be nanometer scale and should be devoid of all pin holes. Covering the porous dielectric material with such a barrier is a challenging task. If the material is highly porous with large pores connected to each other, the barrier may have to be unacceptably thick in order to bridge all the exposed pores. It should be noted that the barrier itself should not penetrate into the porous material, which is a possibility with some deposition techniques. Deposition of an effective barrier is facilitated if the dielectric material used is nonporous.

Good adhesion of the low-*k* material and the barrier layer is one of the prime requirements of a damascene structure. Otherwise, the barrier can delaminate because of the mechanical stresses induced by polishing or thermal cycling. This defect of delamination leads to catastrophic failure in CMP process there by significantly increasing the machine down time and increasing the costs involved to restart the whole fabrication process. Adhesion can also become more of an issue as the porosity of low-*k* materials increases, as increase in porosity decreases the surface area of contact there by decreasing the adhesion strength of the dielectric.

4.7.6. Reliability

There are several issues with the reliability of not just the low-*k* materials, but all the materials incorporated in the modern day IC as they have to survive the typical user environment for significant amount of time without any degradation in performance. However, the porous dielectric materials, especially the polymeric type are considered the weakest links. The thermal conductivity of the materials has an adverse impact on the porosity. Consequently, heat dissipation in the wires leads to increased electro-migration of Cu. There is also a chance of failure of Cu wires by hillock formation as the Cu wires are not firmly encapsulated in dielectric due to the emergence of phenomena of electromigration and diffusion. Furthermore, the thermal conduction mechanism in the newly developed materials needs to be studied in depth to assure the long lifetime of the final circuit.

4.8. Summary and conclusions

In summary, polishing behavior of carbon and fluorine-doped silicon dioxide and other polymer low-*k* materials have been discussed. Nanoindentation studies show that undoped SiO_2 film has the highest mechanical integrity where as spin-on SiOC film shows the lowest. SiLK and xerogel also show very poor mechanical properties. Spin-on SiOC film and SiLK show significant amount of creep due to the polymeric nature of the film. Variation of COF and AE signals has been studied and their variation with machine parameters was discussed. Difference in the variation of the COF for all the films may be caused by their dissimilar interaction of the slurry selective to undoped oxide film and different nature of their surfaces. Undoped SiO_2 film produces highest AE signals among all the films due to the higher interaction of the film surface with the slurry. Material removal for undoped SiO_2, SiOF and SiOC film, grown with standard precursors, follow Preston's equation, whereas for SiOC films grown with non-standard precursors and spin-on method do not follow. Slightly higher removal of materials is found for the films having lower mechanical integrity. AFM surface measurement shows highest surface roughness and maximum height for the undoped SiO_2 film before polishing whereas those are highest for the SiOC spin-on film after polishing. Interaction of slurry on the film surface is due to the reaction with H_2O and OH^- ions and removal of the softer top surface due to the shear of film and pad surfaces. In addition to that it is proposed that material removal from soft films is due to the moving indentation of the hard abrasive particles. Several new generation low-*k* materials have to be porous, soft and polymeric. Hence it is very important to characterize their mechanical, tribological and surface properties. Correlation between performances of CMP with tribo-mechanical properties of these materials will help to understand the fundamentals of the CMP process and optimize it.

5. Cu chemical mechanical polishing

5.1. Introduction: Cu chemical mechanical polishing

The hardness of Cu is significantly lesser than the slurry abrasive particles which are usually alumina or silica. Thus chemical action on Cu to form a harder oxide is essential before mechanical abrasion of Cu. With the all important and decisive role of chemistry in Cu removal, the understanding of electrochemistry and the chemistry in Cu removal gives an insight in to the fundamentals of Cu polishing. In this section, the physical aspects, chemical aspects and defects of Cu CMP are discussed.

Surface layer formation, metal solubility, and metal dissociation can be explained by electrochemistry and dissolution of the abraded material is governed by electrochemical reactions such as:

$$Cu_2^+ + 2e^- \leftrightarrow Cu \tag{5.1}$$

$$2Cu_2^+ + H_2O + 2e^- \leftrightarrow Cu_2O + 2H^+ \tag{5.2}$$

5.2. Copper chemical mechanical polishing

Copper CMP has several important differences to tungsten and aluminum CMP. The hardness of copper (∼1–3 GPa) falls between that of tungsten and aluminum. Thus Cu is easier to abrade than W and can be removed with less scratching than Aluminum. The electrochemical potential of Cu shows

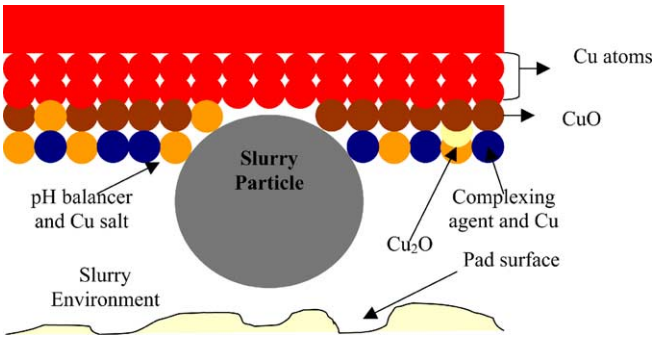

Fig. 100. Schematic of Cu material removal.

that it more noble than Al and W and hence, special slurry action is needed to oxidize Cu without corroding it. When compared with the work of Liang et al. [247] on tungsten polishing, stark differences can be observed and these differences are important to consider in designing and understanding a copper CMP process.

The removal of Cu takes place as follows: (1) dissolution of Cu to form thin few atomic layers thick layer of oxides of Cu; (2) mechanical removal of the abraded material using the slurry particle abrasives; and (3) sweeping away of the abraded material suspended in the solution by slurry flow and pad [56] (Fig. 100).

5.3. Chemical aspect of the copper CMP

The chemical action of the slurry and mechanism of material removal of Cu when polished in a slurry containing fumed alumina (3.1 wt.%) with a median particle diameter of 220 nm, and a commonly used complexing or buffering agent (phthalic acid salt) have been discussed by Hernandez et al. [66]. An illustration synergy of mechanical removal and chemical action where in different copper oxide species exist as a result of increasing and decreasing pH of the reacting slurry have been shown in Fig. 101. As shown by Hernandez et al, when Cu comes in contact with the slurry, complex oxides of Cu comprising of CuO, Cu_2O, compounds of Cu with the buffering agents such as Cu phthalate salts, $Cu(OH)_2$ are formed. The composition of the surface strictly depends upon the interplay of the various species in the slurry. This layer on the surface is then removed using the abrasives in the slurry at the interface between the wafer and the pad and is then washed away with the

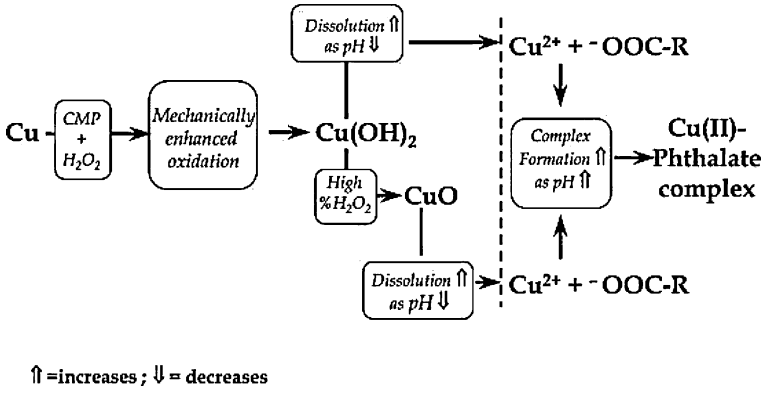

Fig. 101. Summarization of Cu chemical etching and mechanism removal synergy in Cu CMP [67].

slurry. Fig. 100 shows the schematic of complex surface layer formed on the surface of Cu being removed by abrasive slurry particles.

The material removal mechanisms for Cu when polished in different media have also been studied. Tsai et al. [248] have studied the mechanical, chemical, oxidation effect of urea–H_2O_2 slurry medium on Cu using the electrochemical impedance spectroscopy (EIS) technique, while the CMP of Cu in alkaline media have been evaluated by Luo et al. [249]. The effect of slurry on Cu polishing when investigated by Nguyen et al. [250] showed that while static etch of Cu is very low, removal rate of Cu is very high during polishing. This reinforces the theory that there is passivation layer formed on Cu surface which is then removed by the abrasive particles and polishing pad. Thus, the studies indicate the large dependence and variation in the Cu chemical reaction when polished in different slurries [251].

5.4. Cu polishing in acidic slurry

The mechanism of polishing Cu at various dynamic and static polishing conditions in acidic H_2O_2 slurry has been investigated by Du et al. [252] to shed light on the removal mechanism of Cu in acidic medium, something which is not thoroughly understood in spite of large scale research in Cu polishing [166]. Du et al. performed experiments on Cu disks that were thoroughly cleaned using organic solvents and distilled water. Du et al. observed stark difference in the static etch rates and dynamic removal rate of Cu in acidic medium of four pH using H_2O_2 oxidizer. This shows the significant contribution of the mechanical component to the removal Cu during the CMP process. The removal rate increased with increase in H_2O_2 concentration up to a certain point following which there is drastic decrease in the removal rate with further increase in H_2O_2 concentration. This trend is in agreement with previous results [253,254] as the decrease in removal rate is attributed to increase in surface passivation (Fig. 102).

Fig. 103 shows the corrosion current density and the electrochemical potentials measured at different peroxide concentrations. The corrosion current density curve follows a trend consistent with that observed in Fig. 102. Fig. 103 shows that the anodic reaction of Cu is inhibited by increase in H_2O_2 concentration which in turn causes this trend of material removal rate. The increase in passivation causes an oxide layer that inhibits the flow of ionic current there by decreasing the material removal.

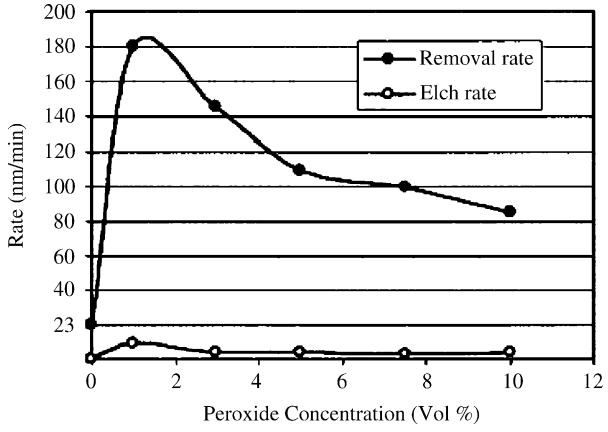

Fig. 102. Change in Cu removal rate with peroxide concentration [252].

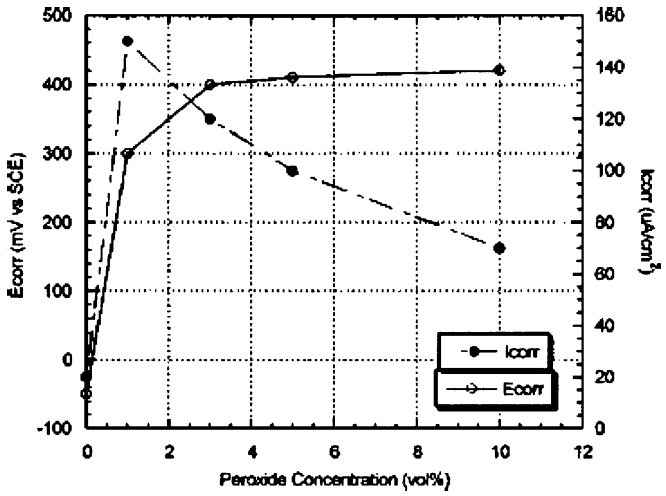

Fig. 103. Effect of H_2O_2 on corrosion potential of Cu [252].

To illustrate the passivation mechanism with regard to time scale, an open circuit potential (OCP) measurement was performed in situ during polishing by Du et al. [252] at different H_2O_2 concentrations. Fig. 104 shows the (OCP) measurements as recorded by Du et al. [252]. The measurements were recorded over a period of 10 min, 2 min after commencement of polishing and restarted after 4 min after the completion of recording. The symmetric curve obtained by Du et al. clearly shows the removal, growth and removal of passive oxide Cu in acidic medium in presence of H_2O_2.

It can be seen from Fig. 104 that there is a dramatic increase in OCP when polishing is stopped for 1% H_2O_2. The increase in OCP has been attributed to growth of the oxide film by Du et al. The sudden decrease in potential once polishing started has attributed to competitive phenomena of growth and removal occurring simultaneously during polishing. For Cu being polished in 5% H_2O_2, the potential jump decreased. It can inferred that this occurrence is due to the comparable rate of passive film formation and removal. This explains the decrease in removal rate with increase in H_2O_2 concentration. The decrease in OCP with further increase of H_2O_2 to 10% shows that rate of film formation is much higher than removal and this explains the further decrease in Cu removal rate.

Fig. 105 shows the variation of surface roughness at diferent aforementioned H_2O_2 concentration as shown by Du et al. It can be seen from the diagram that surface roughness increases (from 1 to

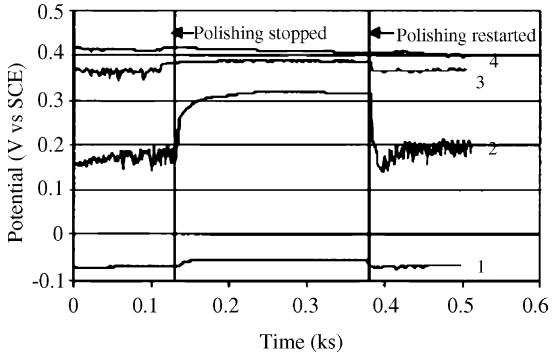

Fig. 104. Open circuit potential (OCP) measurements for Cu polishing in acidic medium for: (1) no H_2O_2; (2) 1% H_2O_2; (3) 5% H_2O_2; and (4) 10% H_2O_2 [252].

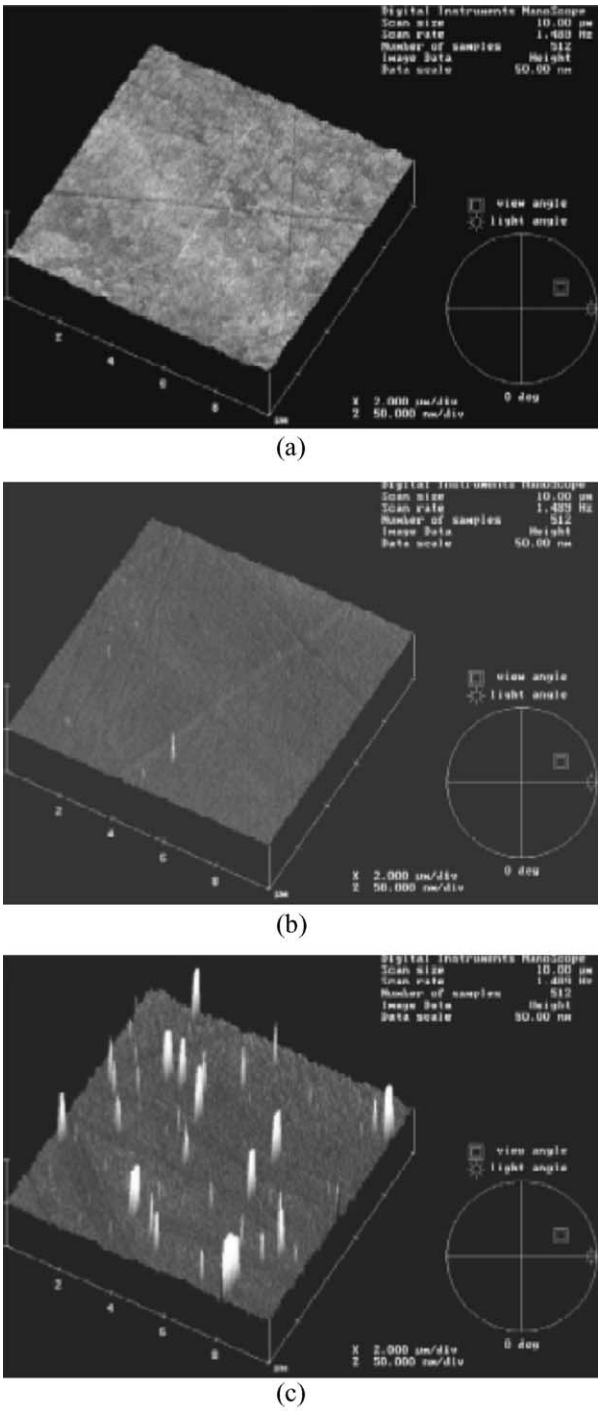

Fig. 105. Variation of surface roughness with: (a) no H_2O_2; (b) 1% H_2O_2; and (c) 10% H_2O_2 [254].

3.1 nm) with increase in peroxide concentration (from 1 to 10%) as the increase in passivating oxide, which is essentially amorphous, considerably increases the surface roughness. This also shows that material removal at high H_2O_2 concentration is essentially mechanical and hence shows lower removal rate. As the surface roughness is also an important aspect of the CMP output parameter, along with

removal rate, it will be advisable to perform the CMP process at 1% H_2O_2 concentration under these conditions of 4 pH as removal rate is compromised when no H_2O_2 is added, thus severely jeopardizing the CMP process effectivity. Based on these results and the X-ray photoelectron spectroscopy of the Cu surface in acidic medium in presence of the H_2O_2 oxidizer Du et al. proposed that for low peroxide concentration, the mechanism of material removal is electrochemical, while for very high peroxide the removal is controlled mainly by mechanical abrasion and in medium concentration of peroxide dual mechanisms exist [252].

5.5. Cu polishing in alkaline slurry

It can be seen from the Pourbaix diagram that Cu can be passivated both in alkaline and neutral medium apart from the acidic medium as discussed above. The use of H_2O_2 as an oxidizer has proved very effective in alkaline, acidic as well as neutral medium [166,254–258]. Ammonium ion is generally used to passivate Cu in alkaline medium as it has the ability to form different complexes with Cu [254–258]. However, the ammonium ion as shown by Steigerwald et al. showed affinity towards the barrier layer as well and hence, the mechanism of polishing of Cu in alkaline medium needs to be further investigated to improve the selectivity of the slurry [254]. Luo et al. [249] studied the effect of ammonium hydroxide on the CMP process and its removal rate. Fig. 107 shows the effect of ammonium hydroxide concentration on CMP removal rate in Strausbaugh 6C CMP polisher as shown by Quo et al.

It can be seen from Fig. 106 that polishing rate is about 130 nm/min when Cu samples are polished without the presence of ammonium hydroxide in the slurry. At ammonium hydroxide concentration of about 0.3 wt.%, the polishing rate increases to about 210 nm/min. Further increase in the concentration of NH_4OH does not have a significant impact on the removal rate of Cu in the slurry when Quo et al. kept the polishing conditions same.

The polarization curves measured with the Struers DAP-V Polisher are shown in Fig. 107 at various NH_4OH concentrations. The Cu-oxide film that is formed on the surface due to the chemical action of ammonium hydroxide is removed by mechanical abrasion. The polarization curves have been measured by Luo et al. [249] during polishing. The leveling-off observed in the anodic branches

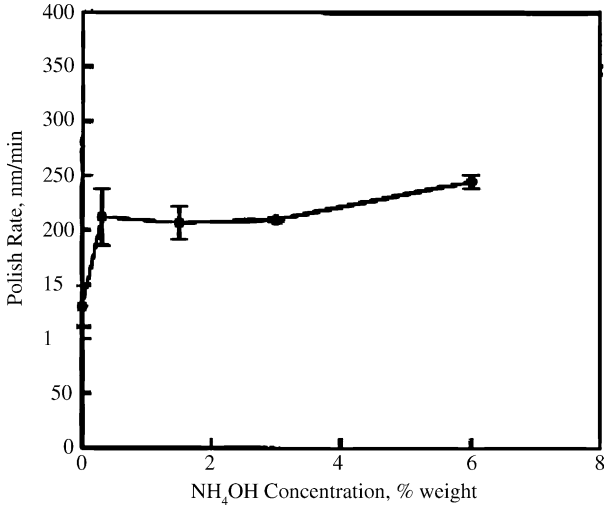

Fig. 106. Effect of NH_4OH concentration on polishing rate of Cu samples [249].

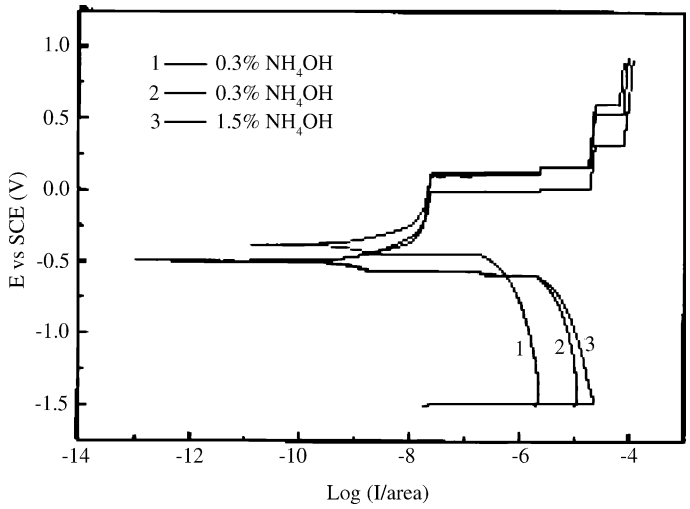

Fig. 107. Polarization curves at various concentrations of NH_4OH measured with the Struers DAP-V polisher. The table speed was 75 rpm and the peed of the disk holder was zero [249].

could be due to the change in the oxidation state of copper from Cu^+ to Cu^{2+}. The OCP, E decreases with NH_4OH concentration from corr 40.3 to 0.9% and remains constant. As shown by Quo et al., the calculated corrosion current density I is only about 1 nArcm, which means that there is a very small part played by chemical action during polishing. This goes on to show that the mechanism of Cu removal mechanism is mainly mechanical due to the slow dissolution rate of ammonium hydroxide as previous shown by Steigerwald et al. [258].

Ammonium hydroxide is known to be a complexing agent and dissolution mechanism has been discussed in literature [259]. The time dependent changes in the low impedance spectrum of the Cu in 1% NH_4OH solution which show the mass transport through the surface layer as shown by Carpio et al. [260] (Fig. 108) are also consistent with the dissolution mechanism and slow rate of dissolution of Cu in ammonium hydroxide as discussed by Harpen et al. previously.

5.6. Cu polishing in nitric acid solution

Ein-Eli et al. [261] studied the electrochemical behavior of Cu in nitric acid solution of 0.2, 1 and 3 vol.% concentration. The potentiodynanmic profiles of Cu samples in nitric acid of different concentration as obtained by Ein-Eli et al. are shown in Fig. 108. Ein-Eli et al. obtained these curves

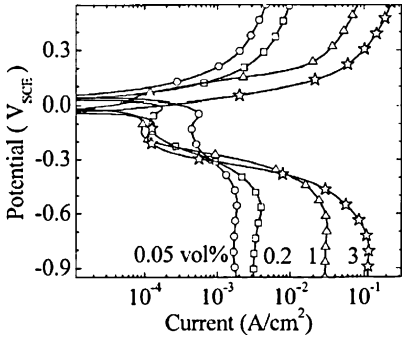

Fig. 108. Polarization curves of Cu obtained at different nitric acid concentration at the scan rate of 1 mV/s [261].

after sustained exposure of Cu samples to the solution. Ein-Eli applied the potential sweep once the steady value of corrosion potential was reached. It can be clearly seen from Fig. 108 that the onset of anodic current was even before any voltage was applied and the current increase with the shift in potential and this indicated active dissolution of Cu in nitric acid. The increase in nitric acid concentration also significantly increased the potential and the anodic current. This showed the vigorous action of nitric acid on the Cu surface with increase in concentration. Ein-Eli et al. observed that the peak of the polarization curve was around 50 mV below the corrosion potential. It also must be noted that the cathodic peak reduces with increase in nitric acid concentration in the data obtained by Ein-Eli et al. Ein-Eli et al. proposed that the aforementioned phenomenon occurs due to the fact that there is a decrease in the amount of precipitants with increase in solubility of Cu at higher

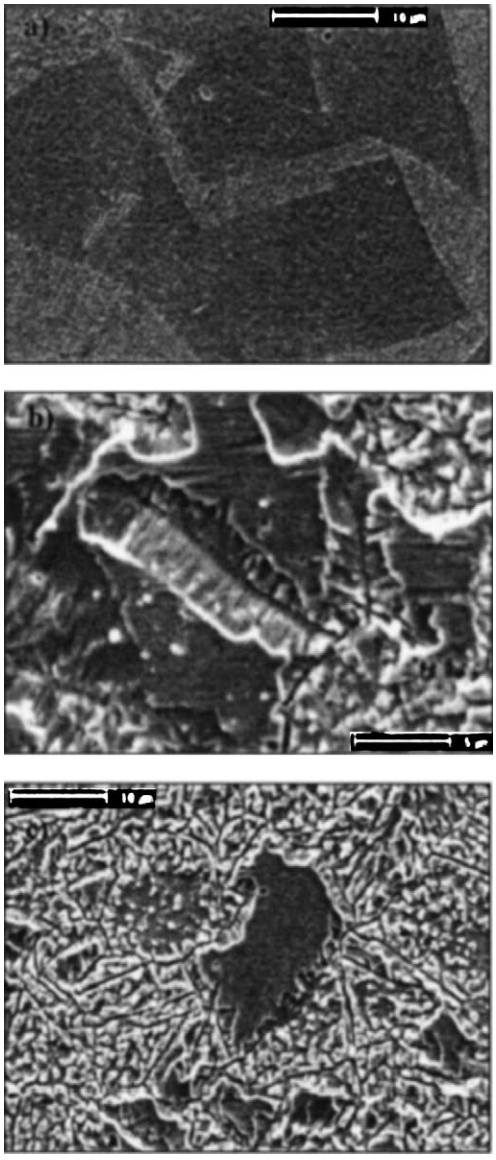

Fig. 109. Scanning electron micrographs of Cu samples in 3 vol.% nitric acid after: (1) 1 min; (2) 1 h; and (3) 1 h at different magnification [261].

Table 24
Corrosion currents, corrosion potential and corrosion at different nitric acid concentration [257]

Concentration HNO_3 (vol.%)	pH	E_{corr} (V_{SCE})	I_{corr} (mA/cm^2)	Corrosion rate (nm/min)
0.2	1.78	0.023	0.604	13.3
1	1.19	0.018	1.658	36.6
3	0.9	0.002	4.468	100.45

concentration of nitric acid. Table 24 shows the variation of corrosion potential, corrosion current with pH and nitric acid concentration [261]. It can be inferred from Table 24 that the corrosion rate of Cu drastically increases with increase in the concentration of nitric acid. This aspect will negatively impact the CMP process due to increase in localized and global corrosion defects. Fig. 109 shows the scanning electron micrographs of corrosion defects with increase in nitric acid exposure. Ein-Eli et al. infer, based on the OCP data that active dissolution of Cu occurs at higher nitric acid solution concentrations, there by rendering it unsuitable to be used in abrasive free CMP.

5.7. *Effect of corrosion inhibitor on Cu polishing*

The addition of corrosion inhibitors like BTA to Cu slurry before polishing is strongly suggested in order to form a protective film over Cu surface and prevents excessive Cu corrosion and dissolution [117,262].

In order to study the effect of corrosion inhibitor during Cu CMP, experiments were performed on: (1) solutions of Na_2SO_4 peroxide-free; (2) Na_2SO_4 with the addition of 0.01 M BTA; and (3) Na_2SO_4 solution containing both BTA ~0.01 M and peroxide 3 vol.% by Ein-Eli et al. [263]. Fig. 110 shows the Cu electrodes polarized in the aforementioned three different candidate solutions as reported by Ein-Eli et al. It can be seen from Fig. 110 that the addition of BTA results in the production of corrosion protective film and there is no increase in current till the potential increase to about 0.25 V, after which there is an increase in current. This increase in current indicates that the dissolution mechanism takes place in Na_2SO_4 slurry after 0.25 V potential. The high resolution SEM micrographs shown in Fig. 111 shows evidence that is in line with this hypothesis. It can be seen from Fig. 111b, c

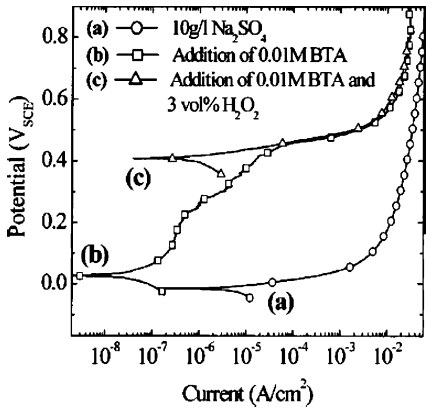

Fig. 110. Potentiodynamic profiles: scan rate of ~1 mV/s of copper electrode immersed in three solutions: (a) solutions of Na_2SO_4 peroxide-free; (b) Na_2SO_4 with the addition of 0.01 M BTA; (c) Na_2SO_4 solution containing both BTA ~0.01 M and peroxide 3 vol.% [260].

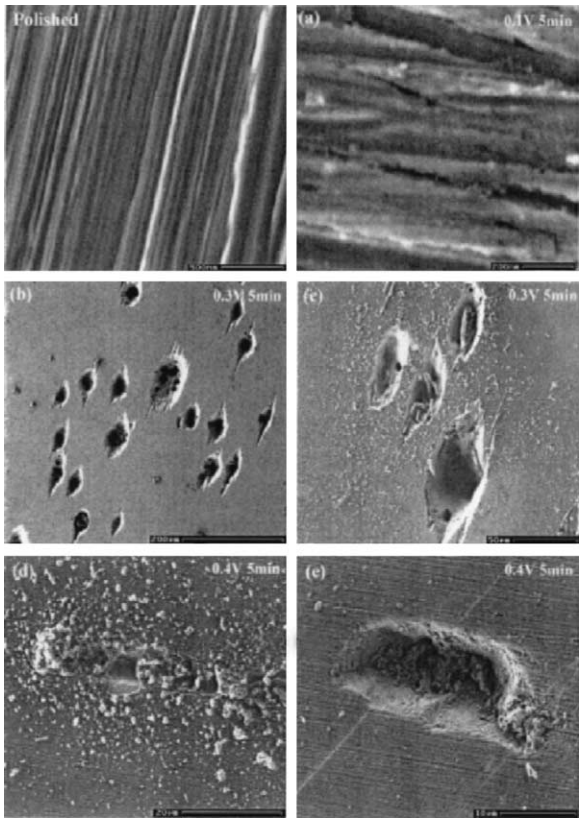

Fig. 111. HRSEM micrographs obtained from copper polarized potentiostatically to: (a) 0.1 V; (b and c) 0.3 V; and (d and e) 0.4 V in solution of Na_2SO_4 containing 0.01 M BTA. Upper left presents pristine polished copper surface prior to immersion in the solution [260].

and d that as compared to the pristine polished samples, when the static polarization of the Cu sample a greater than 0.25 V (in this case 0.3 and 0.4, respectively), there is significant dissolution of Cu and surface damage can be noticed. The same occurrence is not seen in Fig. 111a, where the surface morphology of Cu resembles the pristine polished sample. It can also be noticed from Fig. 110 that

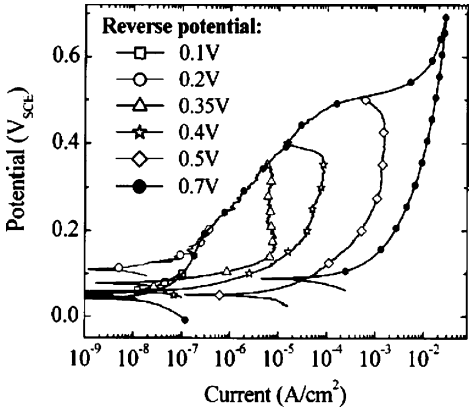

Fig. 112. Potentiodynamic profiles: scan rate of ∼1 mV/s of copper electrode immersed in solution containing Na_2SO_4 and 0.01 M BTA. Copper electrode potential was swept back at potentials ranging between 0.1 and 0.7 V [260].

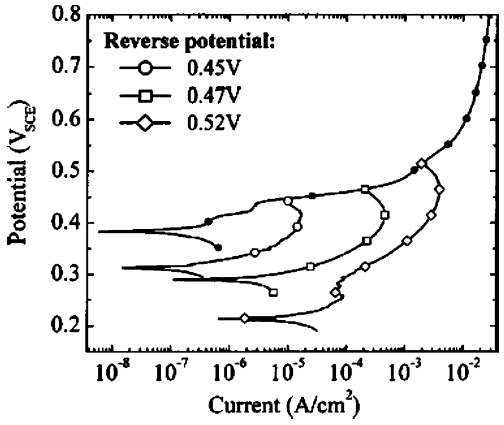

Fig. 113. Potentiodynamic profiles: scan rate of ∼1 mV/s of copper electrode immersed in solution containing Na_2SO_4, 0.01 M BTA and H_2O_2 ∼3 vol.%. Copper electrode potential was swept back at potential of 0.45, 0.47, and 0.52 V [260].

the addition of peroxide solution to the Na_2SO_4-BTA base increases the threshold potential beyond 0.25 V.

Figs. 112 and 113 show the potentiodynamic behavior of Na_2SO_4 solution with (1) just 0.01 M BTA and (2) 0.01 BTA and 3 vol.% hydrogen peroxide, respectively, as reported by Ein-Eli et al. [261]. When the reverse potentiodynamic sweep was applied to solution1, between 0.1 and 0.7 V, Ein-Eli et al. recorded a decrease in current at 0.25 V potential. Ein-Eli et al. proposed, based on the increase in current at the reverse potential above 0.25 V means that the film formed on the Cu surface is not stable above 0.2 V. It can be seen from Fig. 114 that similar results have as seen in the earlier case have been obtained by Ein-Eli et al. with just the difference of threshold potential (0.45 V) in this case. This it can be concluded from the study that addition of corrosion inhibitors to the Cu slurry solution only gives limited protection to the Cu surface.

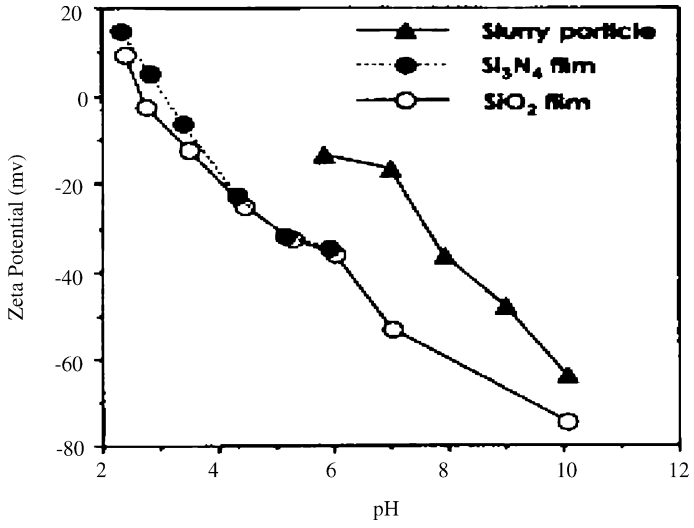

Fig. 114. Change of zeta-potential with pH in SC1 ($H_2O/H_2O_2/NH_4OH$) slurry, SiO_2 and Si_3N_4 films [263].

5.8. Effect of pattern density on Cu polishing

Stavreva et al. [166] studied the effect of the pattern density of Cu CMP process on a commercially available IC 1000/Suba IV pad and QCT 1010 commercial slurry dilute with 3:1 H_2O_2 (30 vol.%). Polishing rates between 300 and 750 nm/min were obtained for Cu-buried SiO_2 at different velocity and down force polishing conditions for the set of pressure and velocity conditions used by Stavreva et al. and rate followed the Preston's equation. The selectivity decreased with increase in removal rate and was found to be inversely proportional to the pressure and velocity, however, sufficient selectivity was obtained to optimize the CMP process. Stavreva et al. performed the unique study of measuring the surface topography as a function of polishing time to investigate the geometry sensitivity of Cu CMP process. It was seen by Stavreva et al. that initially the height difference is equivalent to the polishing rate difference between the high and low areas of the wafer. The polishing difference exists due to the variable contact mechanism and geometry of the pad due to the pattern density variation and height variation in the pattern. However, upon achievement of global planarization, Stavreva et al. concluded, that this difference does not seem to exist. It can be thus inferred that the ''high'' areas of the Cu get polished faster than the low areas, up until the global planarization is reached. However, in case of insufficient Cu thickness, this phenomenon leads to several defects such as dishing and erosion.

5.9. Summary

The effect of machine parameter optimization was discussed in section for silicon di oxide. Cu literature shows that Cu follows the Preston's equation as well albeit with a different constant k. This section elaborately deals with the electrochemical aspect and chemical effects of different slurry solution on Cu surface and its impact on CMP. The fundamental model of Cu CMP has been elaborated and the metal dissolution and removal by abrasion is explained in this section. The effect of acidic slurry and the oxidizer in the slurry on Cu has been discussed in detail. The lowering of removal rate and increase in passivation is observed with increase in oxidizer concentration. Increase in Cu dissolution with increase in nitric acid solution there by leading to corrosion has been illustrated. The influence of corrosion inhibitors in tackling the problem is also documented. The effect of slurry solution and pattern density on defects such as dishing is studied. The inherent weak interface of the certain layers in damascene structure caused delamination to occur during Cu polishing. Low down force polishing and efficient characterization of the interface has been found as the best remedial measures to tackle delamination. The facet of slurry particle agglomeration and its effect on the surface was discussed in Section 3 and has not been dealt with, in this chapter.

6. Post-CMP clean process

6.1. Introduction

As evident from the previous chapters, the process of chemical mechanical polishing, because of the chemical reactions and the presence of abrasive particles at the interface is certain to introduce surface defects and contaminations. The advantages of adopting CMP for global planarization of wafer surfaces will not prove beneficial unless an effective cleaning process follows it. Post-CMP cleaning process is a mandatory step that needs to be carried out in order to ensure a defect free and contaminant free wafer surface for further metallization. Many of the present day CMP equipments are

integrated with post-CMP cleaning unit. Factors responsible for defects and contamination, contaminant retaining forces, theory of particle removal and techniques used for the same are discussed in this chapter.

6.1.1. Factors causing defects and contamination

During the process of CMP of interlayer dielectric (ILD) surfaces and metal layers, surface defects and contaminations are certain to occur. These can either be physical or chemical-based defects and contaminations. Particle defects generate from adhesion of the various particles generated during the process of polishing. These particles can be of the pad material or particles suspended in the slurry. Scratches, voids, grooves, residual slurries and pits are some of the typical surface defects. Another section of defects includes chemical contaminations, ionic contaminations, and corrosion of exposed metal portions on the wafer surface.

These defects cause much damage to the efficiency of the final device. Electrical connections can be affected because of surface defects and voids, which reduce the processing ability for complex calculations. To provide a defect less, planarized surface for further multi level metallization, an efficient cleaning process has to be carried out after CMP process. This chapter explains the theory behind the adhesion of particles onto the wafer surface, inclusion of physical and chemical-based defects, available procedures to efficiently clean the surface and novel proposals and theories for improved cleaning processes.

6.1.2. Contaminations

Contaminations present on the wafer surfaces after CMP process are of two types, particle and metallic contamination. Particle contamination is mainly due to residual particles (of polishing pad) that generate from the abrasion and also retaining of the particles suspended in the slurry. Metallic contamination is observed mainly in the metal CMP process. The chemical metal reactions, electrochemical aspects and the environmental conditions of operation of the polishers are the major factors responsible for metallic contamination. In the following sections the various kinds of contaminations and defects are discussed.

6.1.2.1. Particle contamination. Contamination due to the residual particles left behind by the CMP process is one of the major issues that should be dealt by post-CMP cleaning process. The existence of these particles can be due to many reasons such as suspended particles from various slurries (silica, alumina or ceria), from polished surface materials, from polishing pad and to an extent from the environmental conditions in which the process is taking place. The number of particles on the surface is specific to the process and type of slurry used for planarization, for example, 10^2–10^4 particles per wafer of oxide CMP by wafer when planarized with alumina slurries [65]. Liu et al. [263] demonstrated that the number of particles that get embedded is inversely proportional to the hardness of the wafer surface film. Based on the various surface forces like van der Waals forces and electrostatic forces, particles are absorbed onto the surface. Further in some cases they can be physically embedded onto the surface due to the pressure applied by the polishing pad. These particles need to be removed as quickly as possible. Burdick et al. [264] demonstrated that the adhesion strength of these particles is expected to increase with time [260]. There exists a strong force field at the wafer surface and because of this force field; the wafer surface adsorbs some substances from the surroundings to reduce the surface energy. The adsorption energy is less in the beginning as it is starts with physical adsorption and gradually turns into chemical adsorption. Thus during chemical adsorption particles develop bonding with the surfaces. Thus it becomes very difficult to rinse them off. Liu et al. [265] chose a particular type of highly pure non-ion surfactant in order to ensure that the

adsorption state of the contaminated particle on the surface of the polished silicon wafer remains physical adsorption for a long time. For advanced 0.18-μm technologies the commonly measured particles at 0.2 μm are very close to the line width and thus potentially very dangerous. The SIA road map suggests that back-end processes for 0.18-μm technologies should contribute no more than 50 adders at 0.09 μm for a 200-mm wafer [65].

6.1.2.2. Metallic contamination. One of the major contaminations is metallic contamination. This type of contamination is mainly present on the wafer surface as adsorbed ions, oxides, hydroxides and salts. These metallic contaminants can be removed by wet cleaning procedures using chemicals (acids) such as hydrofluoric acid and citric acid. Further hydrofluoric (HF) is capable of removing metal particles that are present on oxide and nitride surfaces by lift off mechanism better than many conventional solutions and methods of cleaning [65]. As mentioned in the earlier sections of this chapter, these particles generate from the slurries, out cropping of metals on the surfaces, and from the environment of the equipment. CMP processes leave metallic contaminants typically in the range of 10^{11}–10^{12} at./cm^2. In front-end applications (STI), these levels are prohibited because they are not compatible with the various hot processes. In the case of back-end steps, these parasitic metals must be removed, even if this seems more paradoxical with the use of metallization steps. Indeed a large amount of charges at the interconnection level or the presence of mobile ions such as sodium or potassium can induce disturbances during the electrical information transfer. Furthermore, a superficial conductive metallic contamination can generate shorts between two adjacent lines by percolation conduction mechanism. And last but not least, fast diffusers such as copper can reach the active area from the backside surface during the following thermal processes even if performed at relatively low temperature (450 °C). The SIA road map suggests for 0.18-μm technologies that critical metals have to be reduced to below 4×10^9 at./cm^2 for front-end applications and to below 5×10^{11} at./cm^2 for back-end applications [65].

6.1.3. Defects

Apart from contaminations there are other kinds of defects, mostly surface defects. Damaged layer, corrosion defects are some of the surface defects. Surface defects mainly consist of the mechanical abrasion occurred during the CMP process, mechanical inclusions of particles on the surface, chemical effects, etc. These defects are discussed in the following sections.

6.1.3.1. Damaged layer. Damaged layer is one of the surface defects, which is induced during CMP process of wafer surface. The intensity of this damaged layer depends on the type of material and operating conditions of the CMP process. Such a layer needs to be removed as it causes various damaging effects to the wafer characteristics. It presents various undesired effects to properties of the wafer surface like internal stress, and contaminations. The effects of the damaged layer are not yet clearly demonstrated. The thickness of the damaged layer varies typically in the range of 1–10 nm [65]. Such a defect needs to be eliminated during the post-CMP cleaning process, ensuring not to damage the insulating layers or metallic plugs on the wafer surface. This poses a potential challenge while developing the most efficient procedure for post-CMP process. Further care need to be taken not to enhance the already existing defects in the insulator layer such as vertical cracks, surface voids, etc. during the cleaning process.

6.1.3.2. Corrosion effects. Corrosion effects are very critical during the process of chemical mechanical planarization. During planarization of the wafer surface, metal plugs crop up at the surface. Enough care should be taken to ensure that the metal plugs, interconnects are not affected by

the corrosion effects due to the chemical slurries and also during wet chemical post-CMP cleaning processes. The conventional RCA clean cannot be used in such conditions due to the presence of H_2O_2, which is a highly oxidant species. The cleaning process needs to be designed to avoid corrosion, considering the aspects of electrochemistry, which includes the thermodynamic and reaction kinetics aspect. The other important aspect is the photoassisted corrosion. There are chemical agents that can be added to the solution chemistry, which act as corrosion inhibitors. There are two types of corrosion inhibitors, complexing agent or a redox agent. A complexing agent eliminates the free metal ions from the solution and prevents redeposition of metal residue. Addition of such corrosion inhibitors improves the effectiveness of the cleaning process.

6.1.4. Forces responsible for contaminant retention on wafer surface

The force required to remove contaminants and defects from the surface should far exceed the adhesive and various other forces affecting the particle adhesion onto the surface. These other forces are constituted of the electrostatic forces and the capillary forces generated at the interface of wafer surface and the slurry film. The forces of adhesion depend upon a lot of factors like size of the suspended abrasive particles in the slurry, slurry chemistry that induces electrostatic and electrochemical effects, zeta-potential, etc. The section below presents the van der Waals forces and electrostatic forces which constitute the adhesive forces. These forces need to be overcome in order to achieve effective particle removal from the surface.

6.1.4.1. van der Waals forces. As mentioned above, most of the particle contaminants are generated from a combination of sources including particles from the abraded surface, pad material, abrasive particles suspended in the slurry. These particles adhere to the surface as a result of physical attractive forces, between the particles and the surface and also between the particle molecules and the surface, called the van der Waals forces. These are relatively weaker than the chemical bonds. The intensity of these forces depends upon the particle size and the distance between from the surface. Based on the theory, it can be stated that the increasing distance between the particle and the surface results in weaker forces. Also that the decay in the interaction force between the large particle and the surface is slower than the molecule and the surface, and the interaction energy decays at a much faster rate at large separation distances [65]. Inverse variation of this energy can be seen with dielectric constant of the medium used for cleaning. Selecting a high dielectric constant would result in easy overcoming of these forces. This interaction energy has to be overcome by the external forces to remove the particles off the wafer surface to achieve defect free wafer surface.

6.1.4.2. Electrostatic forces. During the process of CMP, wafer and the pad surfaces develop surface charges thereby attracting the ions immersed in the slurry. Two counter layers of charge that develop in the liquid, balance the charge on both the surfaces. This is called double layer. The potential of this layer that forms a boundary for these layers is termed and measured to be zeta-potential. This zeta-potential is a measure of the charge of the layer, which determines the magnitude of attraction or repulsion. Manipulating the pH, electrolytic concentration and adding various surfactants, magnitude of the zeta-potential can be varied. Thus if a high zeta-potential value is maintained, the cleaning process becomes easier. If a large potential with the same sign as that of the particle is maintained, then the repulsion of the particles from the surface is large, resulting in separation of the particle easier removal of the particles and effective cleaning. These electrostatic forces are one of the vital forces that need to be dealt with a clear understanding to achieve high quality cleaning of the surfaces. Liu et al. [263] demonstrated the variation of zeta-potential with increasing pH of the slurry, which has significant effect on the removal of particles from the wafer surface during post-CMP cleaning

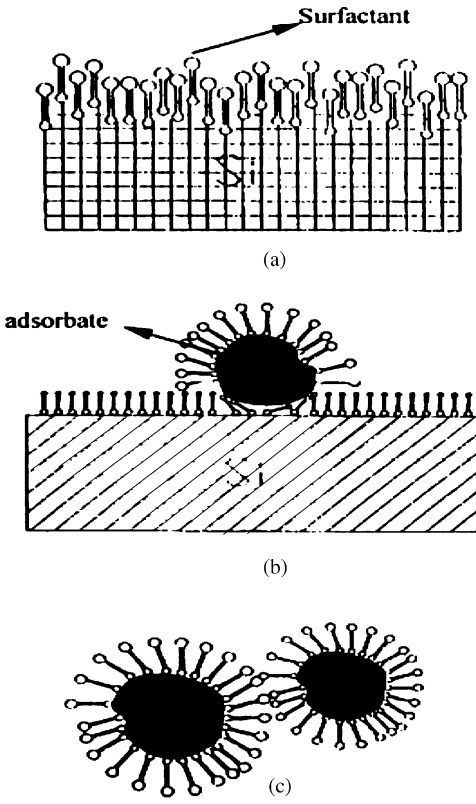

Fig. 115. Control of the adsorption state and removal of the contaminated particle adsorbed on the polished silicon wafer [265].

process. Fig. 115 shows the variation of zeta-potential with increasing pH as demonstrated by Liu et al. [263].

6.2. Theory of particle and contaminant removal

To remove particles, the van der Waals forces first must be overcome to separate the particle form the substrate using mechanical effects such as scrubbing or by chemically etching the particle and/or the substrate to purely and simply eliminate the two surfaces in contact. Harsh accelerations or high-pressure sprays are not able to remove the fine particles. Then the electrostatic interaction must be turned into favorable conditions to avoid particle readhesion. A common practice during post-CMP cleaning is to manipulate electrostatic forces to prevent dislodged particles from redepositioning on wafer surfaces by maximizing the zeta-potential repulsion between the particles and surfaces. Efficient particle removal is extremely difficult because of the wide variety of particulate contaminants and strong adhesion forces. Studies indicate that a combination of cleaning mechanisms is required for efficient particle removal, with a mechanical force being a necessary component in the combination.

6.2.1. Overcoming van der Waals forces

The easiest way to produce a mechanical effect consists of using a brush that is actually brought into intimate contact of the substrate. Other techniques have been recently proposed such as laser flash and shot-peening with argon or ice microballs but they are still not yet developed enough for

consideration. In the case of underetching removal process, one of the main parameters is the etching thickness. On silicon, a 2-nm etching is necessary to remove the particles. This distance corresponds to a theoretical decrease of the van der Waals interactions of about three orders of magnitude, but 4–5 nm underetching seems to be more appropriate for oxide cleaning. Furthermore the optimal removal efficiency does not seem to depend on the etching rate, unlike what could be expected from the dynamic aspect of the redeposition process. As seen 3–4 nm under etching is necessary in the case of silicon nitride. The hydrodynamic forces that can be generated during the removal mechanism also aid in the particle removal to a great extent. Zhang et al. [266] evaluated the adhesion forces that retain the contaminant particle on the surface and the hydrodynamic forces that are generated to estimate the removal mechanism efficiencies. The surface of the wafer, which becomes unstable due to the force field, adsorbs some substances to decrease the surface energy [265]. This adsorption starts as a physical adsorption and later develops into a chemical adsorption, which results in holding the adsorbed substance more firmly. Liu et al. [265] stated the use of a highly pure non-ionic surfactant to lengthen the period of physical adsorption, where in the removal of the substances is relatively easier compared to the chemical adsorption. Fig. 115 demonstrates the effect of surfactant.

6.2.2. Prevention of electrostatic readhesion

The second step consists of preventing the readhesion of the just-liberated particles by annihilating the electrostatic attraction forces between the substrate (scrubbing brushes when used) and the particles or even better by obtaining a repulsion force. The charges are usually mainly located at the particle or substrate surface. Their origin is generally due to the chemical terminations of these surfaces. These terminations are in equilibrium with the solution and can therefore be modified by the pH or by some species, to a certain extent in the same way as ion exchange resins. The surfaces of charged particles or substrates dipped in aqueous media are immediately surrounded by a layer containing an equivalent but opposite charge of ions from the solution. The zeta-potential plays a very vital role here. It can be manipulated by changing the pH as mentioned in earlier sections, thus resulting in the repulsion force between the surface and the adhering particles.

6.2.3. Effect of zeta-potential

The zeta-potential depends on the pH of the chemical solution used for cleaning. Liu et al. [263] demonstrated (Fig. 116) that the particle level on the wafer surface reduces with increasing pH. The zeta-potential is also modified by the ionic strength. Absolute value of the zeta-potential reduces as the ionic strength increases. This observed phenomenon could be explained by both the presence of more counter ions in the shear layer due to the decreasing double layer thickness and to the increasing counter ion adsorption into the stern layer [65]. The electrostatic interactions between the substrate and particles are eliminated at a smaller distance in the case of a thin double layer (high ionic strength), which leads to a better removal efficiency. Fig. 116 shows the decrease in the number of particles on silicon oxide and nitride films with increasing pH.

6.3. Procedures for post-CMP clean

Procedures for the post-CMP cleaning process are developed and are already in use. Major procedures that are practical and are being used in the current industry are discussed here. A variety of procedures are available from which the most optimum, both performance wise and taking economical aspects into consideration are chosen based on the level of purity that is needed to be achieved and the amount of contamination that is expected out of the slurry composition and properties of the surfaces.

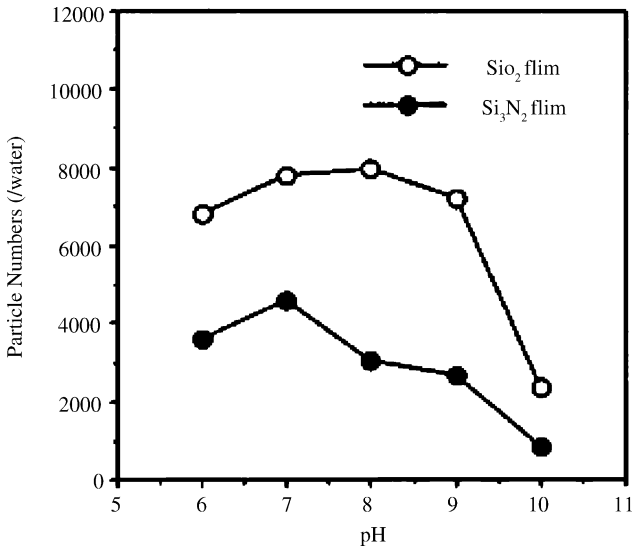

Fig. 116. Particle numbers on SiO_2 and Si_3N_4 films immersed in various pH solutions for 30 min after CMP process [263].

6.3.1. Brush scrubbing mechanism

This is one of the oldest and effective methods for removing particles from wafers. The mechanical force component of the material removal force is provided by the brush bristles. In this mechanism, brushes are used on single or both sides of the silicon wafer to scrub the surface thereby removing the particulates on the surface of the wafer. These brushes are typically made of polyvinyl alcohol (PVA) material, the texture of which is soft when wet. In spite of the name, it uses hydrodynamic drag to exert a removal force on the surface particles. Deionized water is typically used to generate electrostatic forces between the wafer surface and the dislodged particles to prevent the redeposition of those particles. Zhang et al. [267] carried out statistically designed experiments and stated that brush–wafer separation distance, brush down force (which is related to brush compression), brush rotation speed significantly affect particle removal during brush scrubbing. A relationship between brush compression and removal efficiency exists and indicates that hydrodynamic forces alone may not be responsible for particle removal during brush scrubbing [264]. In some situations brush bristles do not contact the particle or the surface but rather act as oars or paddles that push liquid across the wafer surface, dislodging particles. Such a technique of not making a physical contact is effective for relatively larger particles (>1 μm) [264]. As it does not come in direct contact, it is suitable for both hydrophilic and hydrophobic wafers. In case of smaller particles (less than 1 μm) brush-particle contact needs to occur for complete particle removal, as the hydrodynamic drag would not be sufficient to remove all the adhered particles which have greater van der Waals forces or sometimes get physically embedded into the surface because of the contact pressure during CMP. Figs. 117 and 118 show the schematic of single sided and double-sided brush scrubbing mechanisms. The radial distances and the angular velocities determine the linear relative velocity between brush and wafer. Burdick et al. [264] used these parameters to develop the equations for particle velocity as a function of relative velocity between the brush and wafer, which were further used in hydrodynamic modeling of the cleaning mechanism. Even though this is the major cleaning process available in the industry, this process has a major limitation of cost of ownership. As this process cannot clean a batch of wafers at one time and because of the limitation of life of the brush, the process is expensive. Moreover the economic studies state that this process is three times more expensive than the wet

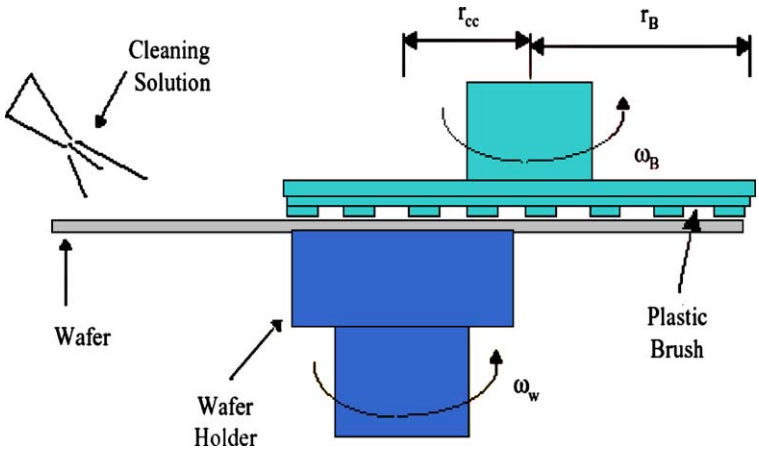

Fig. 117. Schematic of single sided brush scrubbing mechanism: r_{cc}, offset distance; r_B, brush radius; ω_B, brush angular speed; ω_W, wafer angular speed [267].

cleaning process [65]. Ramachandran et al. [268] have evaluated the brush scrubbing mechanism for post-CMP cleaning of thermal oxide wafers. Scrubber optimization was performed by adjusting various parameters like brushes, wafer rotation speeds, DI water flow and the brush height. They also stated that the removal efficiency does not vary a whole lot with respect to the variation of brush speed, although at higher speeds the removal is demonstrated to be marginally better. Brush must typically be compressed 2–3 mm onto the wafer surface to come in direct contact with the wafer, which represents the only way to remove the fine particles due to the weakness of drag forces. In the case of tungsten or copper CMP where alumina slurries are used, the pH of the solution must be greater than 9 or lower than 2 to avoid adhesion of the slurries in the porous structure of the brush [65]. This phenomenon, called the loading effect, if not prevented, increases the final particle levels on the wafers and therefore

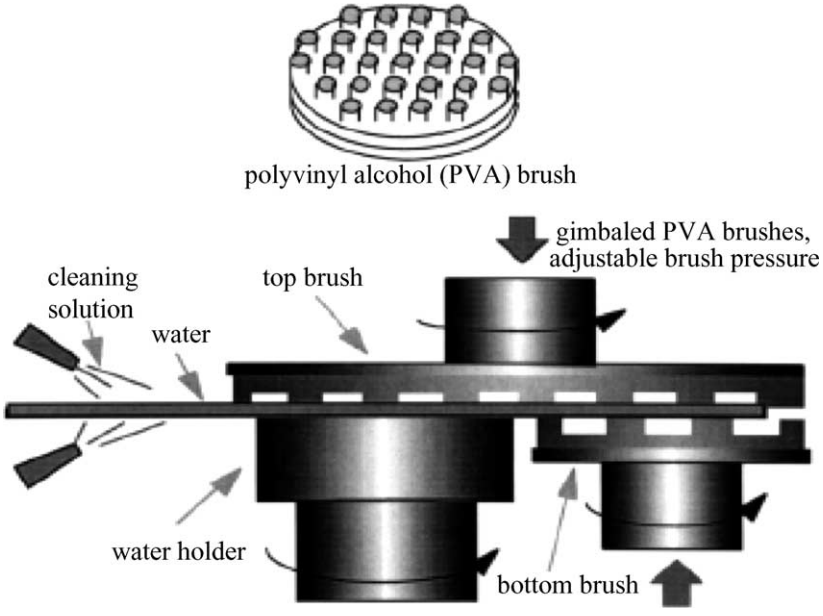

Fig. 118. Schematic of double sided brush scrubbing unit [267].

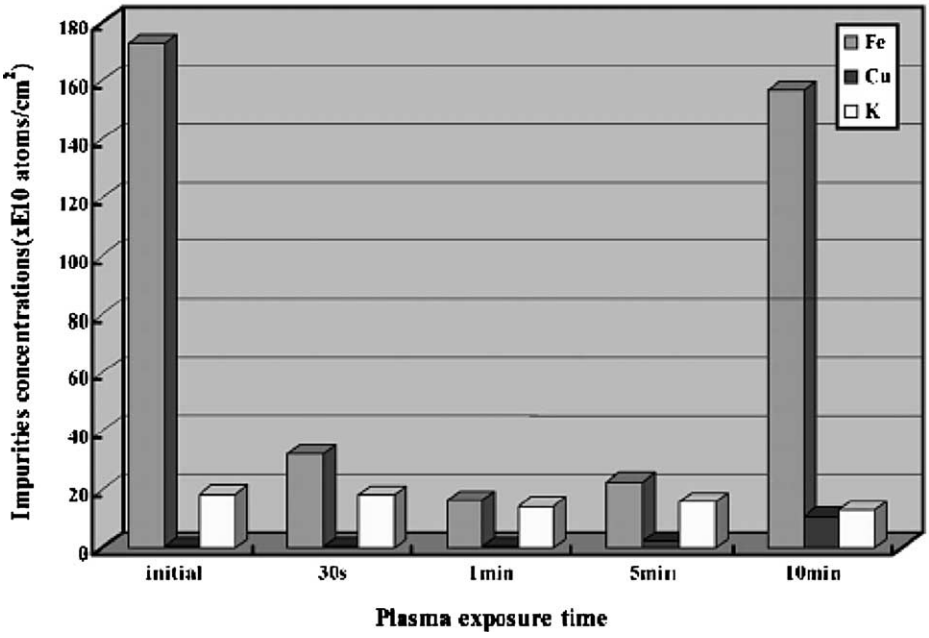

Fig. 119. Effects of the plasma exposure time in the remote hydrogen plasma cleaning process on the metallic impurities removal [269].

drastically reduces the brush lifetime. This effect can be greatly attenuated by injection of chemicals to vary the pH, for example, injection of 0.5–2% ammonia.

Lim et al. [269] developed a dry cleaning process as a second step for removal of metallic contaminants like Cu, Fe and K after brush scrubbing mechanism for cleaning of oxide and metal CMP. They carried out post-CMP cleaning using remote plasma hydrogen cleaning and UV/O_3 cleaning process. Fig. 119 shows the variation of metallic impurity concentration on the surface with the plasma exposure time.

6.3.2. Chemical wet cleaning

Chemical cleaning is very significant in post-CMP cleaning process. It has the advantage of low cost of ownership and high throughput as several wafers can be cleaned simultaneously in batches, unlike brush scrubbing mechanism. Tardif et al. [270] developed various cleaning chemistries for cleaning of PECVD TEOS oxide. They used 0.1% HF, BOE 1/80 diluted 30 times, BOE 1/80 + NH_4OH + H_2O [1, 0.05, 100] 63 °C diluted NH_4OH [0.25, 6] 55 °C for 10 min. Fig. 120 demonstrates the performance of varying scrubber chemistries. Fig. 121 presents a comparison of scrubber performances with cleaning solutions to only cleaning solutions. Slurry residues can be removed using wet chemistries in both acidic and alkaline media.

Both alumina and silica slurry residues on oxide film can be removed using the standard SC1 ($H_2O/H_2O_2/NH_4OH$) solution and SC1 without water peroxide can be used for tungsten cleaning. In the absence of water peroxide, OH^- species will roughen the silicon surface by etching it, as there is no protective layer formation. To prevent this, backside of the wafer should be coated with nitride or an oxide layer [65,271]. Using acids like HF present a good cleaning chemistry, as it does not affect the back-end layers and barriers. The absolute pH of these acidic solutions is less, making the particle and residue removal difficult to achieve. High power megasonics should be employed along with these chemical treatments to achieve as good as efficiency with the scrubber mechanisms [65]. These wet

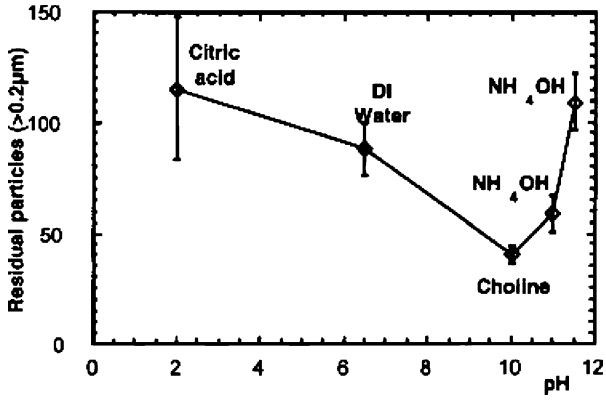

Fig. 120. Performances of different scrubber chemistries in terms of residual SiO_2 slurries intentionally deposited on thermal oxide [270].

cleaning chemical treatments, even though with a lesser efficiency when compared to the scrubber mechanism, present a cost cutting alternative for brush scrubbing post-CMP cleaning process.

In spite of many advantages of Cu to be used for interconnects and effective CMP of Cu, Cu CMP induces many surface residues and organic residues from benzotriazole, which is used for enhanced CMP process. These residues result in Cu ion drift, which degrades the dielectric surface arising reliability issues. A suitable post-CMP cleaning step is extremely necessary after CMP pf Cu surfaces. Benzotriazole is usually used to achieve good wafer planarization, which induces organic contamination. Main challenge of Cu CMP is removal of Cu residue and BTA contamination from inter-metal dielectric layers and Cu surface. Yeh et al. [271] developed a novel cleaning process using buffered HF solution and ozone water for Cu post-CMP cleaning process. A buffer hydrofluoric (BHF) cleaning solution, HAL 4006 and HAL 4025 were used to reduce Cu and BTA contaminations on the IMD surface. Ozone water immersion step followed the main buffered HF solution cleaning for further cleaning.

Wang et al. [272] developed a modified multi-chemical spray process for post-CMP cleaning application. This new process has been successfully applied to both oxide and tungsten CMP cleaning. They used ammonia/peroxide mix (APM), dilute HF dip (for intermediate short step) and hydrochloric peroxide mix (HPM) chemistries for cleaning. They also used a various combinations of these three

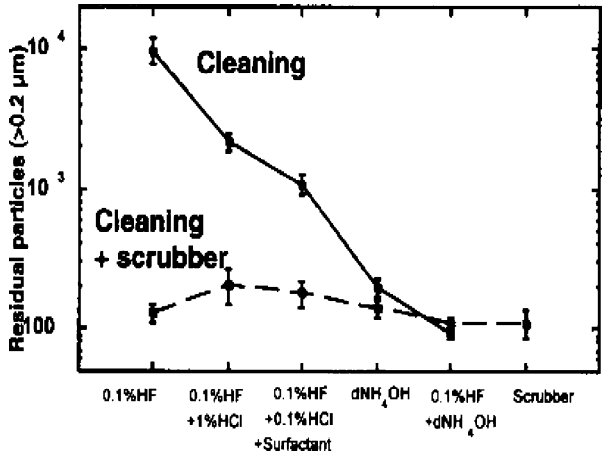

Fig. 121. Comparison between scrubbing and different wet chemistries in terms of SiO_2 slurry removal efficiency [270].

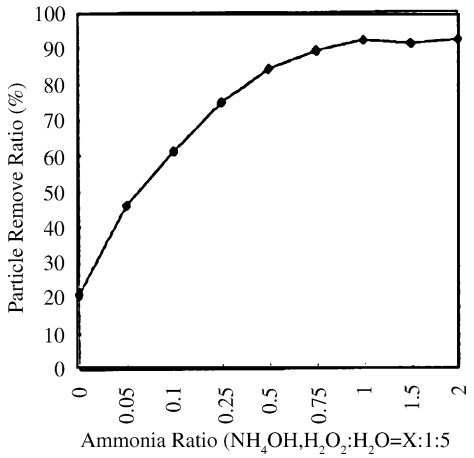

Fig. 122. The particle removal ratios for different cleaning NH_4OH ratios [271].

solutions to achieve better results. Their procedure works according to the fact that when the zeta-potential between the slurry particles and wafer surface are all the same sign, it will be easier for the particles to be removed from the wafer surface due to the electrical repulsive forces. The effect of pH and zeta-potentials when using NH_4OH and H_2O_2 is believed to be the critical factor improving the removal efficiency. This is particularly useful for post-tungsten CMP cleaning as there are low pHs involved in the process of CMP of tungsten, which uses alumina-based slurries. They demonstrated that these chemical-cleaning combinations could achieve comparable levels of cleaning with brush scrubbing cleaning mechanism. Fig. 122 shows the increase in percentage removal of particles using APM and extended combinations.

6.3.3. Hydrodynamic jets and spin-rinse drying

Hydrodynamic jet cleaning is basically impinging pressure jets on the wafer surface, which removes particles by hydrodynamic drag. There are low pressure and high-pressure hydrodynamic jets that are used for cleaning. Even though theoretically high-pressure jets are expected to remove particles more effectively, low-pressure jets are typically used to avoid wafer surface damage. This process is more effective for small particles than micron size particles [65]. This type of cleaning is more effective than mechanical brush scrubbing in case of small particles (sub micron). For micron size particles, the pressure to remove them is more than sufficient to damage patterned surfaces. Hydrodynamics play a major role in these types of mechanisms. Burdick et al. [273] have developed a numerical model, which describes the effect of hydrodynamics on the particle removal. They developed a model based on the critical Reynolds number, which is independent of particle size. In some cases, spin-rinse drying is used wherein the particle and chemicals on the surface are removed by centrifugal force along with the application of low-pressure sprays.

6.3.4. Megasonic acoustic cleaning procedure

Ultrasonic and megasonic cleaning is an evolving technique for post-CMP cleaning process. This involves introducing frequency pressure waves in a cleaning bath using acoustic transducers. Megasonics is proven to be more effective than ultrasonics in sub micron range and it prevents defects like cavitation. In addition of the physical megasonic effect in removing particles, the use of chemistry has shown big improvements in cleaning efficiency. Megasonic cleaning efficiency depends on various parameters like power, length of cleaning and different temperatures. Moumen and

Busnaina [274] investigated the parameter effects on efficiency of megasonic cleaning. They concluded that high efficiency could be achieved with high megasonic power, long cleaning times and at high temperatures. Megasonic post-CMP cleaning process was demonstrated by Busnaina and co-workers [274,275]. Very efficient removal of particles was demonstrated using acoustic streaming in combination with SC1 solution. Dilute chemistry was used to enhance particle repulsion, removal and prevent redeposition. Also their results show that using dilute SC1 reduces the cleaning time as compared to DI water.

6.3.4.1. Dry cleaning non-contact cleaning process. Researchers at Phrasor Scientific Inc. (Duarte, CA) have developed a noncontact wafer cleaning technique namely NanoClean [276]. This method can remove sub micron debris and particulates from surfaces in a single step. This method requires no rinsing or drying steps. They generated high-energy beams of microclusters directly from liquid state, which have an average size of less than 1 micron. They described that when the clusters meet the submicron particles on the surface, momentum of the clusters gets transferred to the particles, which eventually results in their removal. The forces imparted by these clusters are sufficient enough to remove the particles physically from the surface. These clusters gain supersonic velocities as they are accelerated electrically. Regulating the velocities and direction of motion of the clusters would eliminate the possibility of damage occurring to the surface. This precision cleaning process can be used to supplement to the conventional wet cleaning or brush cleaning process that are already existing in the industry.

6.4. Summary

Post-CMP cleaning has evolved into a significant process as CMP introduces several defects and contaminants. To achieve a wafer surface free of defects and contaminants, a thorough understanding of cleaning mechanisms, forces involved, electrochemistry, hydrodynamics and colloidal sciences is highly necessary. Brush scrubbing mechanism in conjunction with chemicals is currently employed in the industry. To optimize cost of ownership, novel techniques are being developed by several researchers. Wet cleaning methods (using combination of chemicals) and acoustic streaming techniques are being developed. Many researchers have demonstrated the comparable performance of various alternatives to the currently existing brush scrubbing mechanism. Using various chemical solutions in combinations to achieve an optimum pH for the cleaning solution plays an important role in cleaning process. This section of the report is aimed at providing the details of post-CMP clean including the procedures and the recent advances in the industry. Research for novel techniques should be carried out continuously to follow the planarization of new materials. Novel techniques are being developed and much advancement is yet to take place to find competing alternatives to the existing methodologies. Success and advantages of CMP highly depends on the efficient cleaning process. Research in post-CMP process plays a vital role in the advancements taking place in the field of IC fabrication.

7. Conclusion

7.1. Summary

The paper begins by stressing the importance of research in the STI and BEOL processes. It discusses the need for planarization and different techniques of planarization. It can be seen from the

discussion that the technique of chemical mechanical polishing offers tremendous benefits over the other available techniques at present. The technique of CMP is especially suitable for shallow trench isolation of devices and fabricating dual damascene structures for interconnects. The paper tries to understand the exact science of the CMP process. The mechanism of material removal and planarization strictly depends upon the material that is being removed. The CMP process has different material removal mechanism and surface tribochemical interaction for silicon di oxide, polymers, metals and ceramics. The different efforts for the theoretical characterizations of different surface interactions have been mentioned in the paper. The paper gives a brief outline of the physical process of CMP and industrial standards that are followed while performing different CMP processes at different times during the semiconductor device fabrication. The dependence of the CMP process, its surface chemical reaction, abrasive wear and the associated output parameters such as removal rate, global planarization, uniformity, surface roughness, etc. on the input variables such as spindle speed, down force, slurry flow and platen rotation has been discussed at length in the paper. Consumables form an important part of the overall CMP process. The paper presents a review of the various pads, different types of slurries, retaining rings and other consumables available in the market and under research at this time. The consumable parameters such as pad porosity, hardness, elasticity, slurry pH, slurry chemistry and its effect on the CMP process parameters such as removal rate and process defects have been reviewed. The paper goes in details of the different CMP process employed to polish dielectrics, metals and ceramics. The various issues that arise during the polishing of various doped and un doped oxide, soft and inherently weak polymeric materials used as dielectrics, novel aerogels and xerogels presently under consideration for implementation as future dielectrics have been discussed at length. The paper also dwells on the CMP of tungsten plugs, Cu and Al interconnects, as well as Pt CMP for some specialized application. The post-CMP issues such as particle adhesion, corrosion and surface scratches have also been discussed in the paper.

Due to the implementation of novel thin films in the integrated circuits, the issues such as weak interfacial adhesion are influence the CMP of these materials a lot. The weak interface gives rise to a catastrophic failure of the polishing thin film known as delamination. The material that is being polished also can have a lot of micro scratches as at the end of a CMP process. Due to agglomeration of smaller particles in the slurry, a large chunk of particulate materials comes in contact with the slurry there by causing the microscratches to occur on the surface. Dishing reduces the final thickness of copper lines and degrades the planarity of the wafer's surface, resulting in complications when adding multiple levels of metal. Understanding of dishing and its nature will be very helpful in process optimization and helps to understand the process mechanism. Erosion is the thinning of oxide and metal in the patterned area. By definition, it is the difference in the SiO_2 thickness before and after polishing. The pattern density dependant defects of dishing and erosion are also vigorously being studied by the semiconductor industry today. The process optimization issues such as lowering the within and across-wafer polish rate non-uniformities to achieve the required statistical process control metrics and effective process end point detection have been discussed.

The process defects in CMP occur not only during the actual polishing but also during the post-CMP clean operations. Defects like metal corrosion occur as the wafer is cleaned in highly voracious post-CMP clean environments. The paper talks in brief on the various post-CMP clean mechanisms presently being employed and the on going efforts to minimize the defects that occur on the wafer during the post-CMP clean process.

Post-CMP metrology is very important to determine the accuracy and reliability of the CMP process. The integrity of the surface and pattern has to be accurately determined and evaluated. This paper presents and overview of the various metrology techniques that have been implemented to evaluate the CMP process and polishing behavior of the various CMP consumables.

7.2. Out line of future trends

There are several innovations and modifications such as slurry free approach, low down force polishing, abrasive less and nanoparticle slurry approach, etc. that are being carried out in the CMP process. Process such as reverse electroplating and combination of different planarization process, are also trying to compete with CMP for achievement of effective global and local planarization of the wafer.

CMP has evolved into one of the most significant process in circuit fabrication. In the circuit fabrication device isolation plays a significant role in improving the performance of the devices. Device isolation is made possible by shallow trench isolation method, which replaced local oxidation of silicon (LOCOS) in the recent times. STI allows scaling down the device dimensions and more dense packing. CMP of the deposited insulator over the etched transistor active area during STI is necessary. STI is one of the many technological advances in the recent times, which supports shrinkage of the device dimensions. STI provides a good prototype for CMP, which will be carried out for many such advances.

The process of chemical mechanical polishing is also finding increasing application in the field of giant magneto resistive (GMR) and colossal magneto resistive (CMR) disc drives for polishing successive layers of thin films (Co and Ni). Special emphasis is laid on successful endpoint detection and selectivity of the slurry. CMP is used to polish multi-level thin film structure of the drives.

The field of microelectromechanical systems (MEMS) is also increasing adapting the process of CMP. As MEMS structures implement smaller and smaller features as constituents, the planarity of the thin films becomes an important issue. For optical MEMS applications the mirror like smooth surface of the thin films is of utmost importance for reliable and repeatable functioning of the device, for example, optical features.

Metal and high-k insulators have replaced the dummy gates, which were used to preserve self-alignment of gate electrode. These metal and insulator layers need to be planarized with utmost control, where CMP has to play a significant role. Deposition techniques for such metal and high-k insulator films are yet to be defined and CMP of films deposited by such atomic layer depositions need to be investigated to get optimum polishing performance. Also, CMP of noble metals, which are used to make gate electrodes in p-channel devices need to be investigated to achieve optimum removal performance.

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