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Mechanical Reliability and Characterization of Modern Microelectronic Interconnect Structures

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Abstract

As there is a need to increase the number of transistors while lowering chip dimensions and reducing power consumption, there have been sudden changes in the materials used in modern microelectronics applications. Aluminum interconnects in the microelectronic devices have been pushed to their dimensional limits due to reliability problems. Copper, having a higher conductivity and better electromigration properties is replacing aluminum in integrated circuits. It is also beneficial to use a material with the low dielectric constant (K) to fill the space between Cu interconnect lines in order to reduce the amount of cross talk between interconnects and place them closer to each other. The difficulties of poor low-K dielectric materials and copper adhesion, as well as Cu diffusion into a silicon substrate have been challenging, but were overcome by Motorola, as well as other IC manufacturers. Nanoindentation is a powerful technique for measuring mechanical properties of thin films. First applied over 20 years ago in the hard drive industry, it is now commonly used for other applications. This paper describes advanced interconnect materials characterization along with nanoindentation techniques for measuring thin films mechanical properties, including elastic modulus, hardness, adhesion and fracture toughness as applied for modern microelectronics reliability.

Author Biography

Dr. Alex A. Volinsky obtained his PhD from the University of Minnesota, Chemical Engineering and Materials Science Department in 2000. He currently holds a Senior Member of the Technical Staff position in Motorola Digital DNA^{TM} Labs, being in charge of the X-Ray characterization laboratory, part of the Process and Materials Characterization Lab (PMCL).

Introduction

Rapid growth in the microelectronics industry for the past several years requires very fine interconnects with thin metal lines within one chip. A modern integrated circuit (IC) contains more than 200 million transistors. There is a need to increase the number of transistors while lowering the chip's dimensions and reducing the power consumption. Aluminum interconnects in the microelectronic devices have been pushed to their dimensional limits due to reliability (electromigration and stress migration) problems. Copper, having a higher conductivity and better electromigration properties is replacing aluminum in integrated circuits. It is also beneficial to use a material with the low dielectric constant (low-K) to fill the space between Cu interconnect lines in order to reduce the amount of cross talk between interconnects and place them closer to each other. Basically, it is the whole materials system that has been changed with the introduction of Cu metallization.

The difficulties of poor low-K dielectric materials and copper adhesion, as well as Cu diffusion into a silicon substrate have been challenging, but were overcome by Motorola, as well as other IC manufacturers. The device reliability depends on many factors including materials ability to withstand intrinsic device stresses, the materials adhesion to its neighboring structures, requiring a thorough study to ensure the IC mechanical reliability. For the mechanical reliability four materials properties are important, namely thin film elastic modulus, yield stress, fracture toughness and adhesion. All these properties can be measured by means of nanoindentation techniques.

Modern Cu/low-K vs. Al/SiO_2 technology

Al and Al alloys are the most common materials for interconnects in very large-scale integrated (VLSI) devices. However, these materials, due to the relatively low melting point of Al, are susceptible to stress and electromigration, which confines interconnects dimensions by a certain limit. Current density in interconnects can reach values of $1\text{-}2\cdot10^5$ A/cm^2 during device operation at 125 °C [1]. Electrical conductivity of copper is 5.88 $(\text{ohm}\cdot\text{cm})^{-1}$ as compared to 3.65 $(\text{ohm}\cdot\text{cm})^{-1}$ for aluminum [2], which means that for a given cross section of a metal thin interconnect, copper can transport more charge. At the same time thermal conductivity at room temperature is 4.01 $\text{W}\cdot(\text{cm}\cdot\text{K})^{-1}$ for bulk copper and 2.37 $\text{W}\cdot(\text{cm}\cdot\text{K})^{-1}$ for aluminum. After serving the microelectronic industry for over 30 years, Al is being replaced by Cu. The transition has not been smooth though, and took almost 10 years of research and development work.

Al has a very dense native surface oxide, which prevents further Al oxidation and diffusion, and promotes adhesion as well. Opposite to alumina, copper oxides are not dense, porous, and do not protect the metal surface from further oxidation. In fact, Cu is known to oxidize at room temperature. Copper diffuses into silicon, reaching active layers, which makes devices inoperable. Unlike Al, Cu does not adhere well to semiconductor substrates. Barrier layers have been used with Al interconnects to improve reliability, microstructure and processing, reduce grain size, improve (111) Al texture and decrease line resistance. In addition, for the Cu technology, a barrier layer is essential to prevent copper diffusion and enhance adhesion.

It is also beneficial to use materials with the low dielectric constant (low-K) to fill the space between Cu interconnect lines in order to reduce the amount of cross talk between interconnects and place them closer to each other. Basically the whole manufacturing process had to be changed with the introduction of Cu metallization.

For the classical Al technology, barrier layers and Al are sputter deposited and patterned using lithographical techniques (Figure 1). The space in-between the interconnect lines is filled with SiO_2

(dielectric constant of 4.2). The process is repeated for the consequent layers. A side view of an Al line on top of SiO_2 is shown in Figure 2a with individual Al grains seen at the top.

For the modern Cu technology the trenches are patterned first, and then Cu is electroplated on top of the sputter deposited barrier and Cu seed layers (Figure 1). Excessive Cu is removed by the Chemical Mechanical Planarization (CMP) process. While CMP can also be used with the Al technology, Cu layers are typically much smoother, which allows for a larger number of metallic layers in the device, thus higher complexity and level of integration. An SEM image of the Cu line cross-section is shown in Figure 2b.

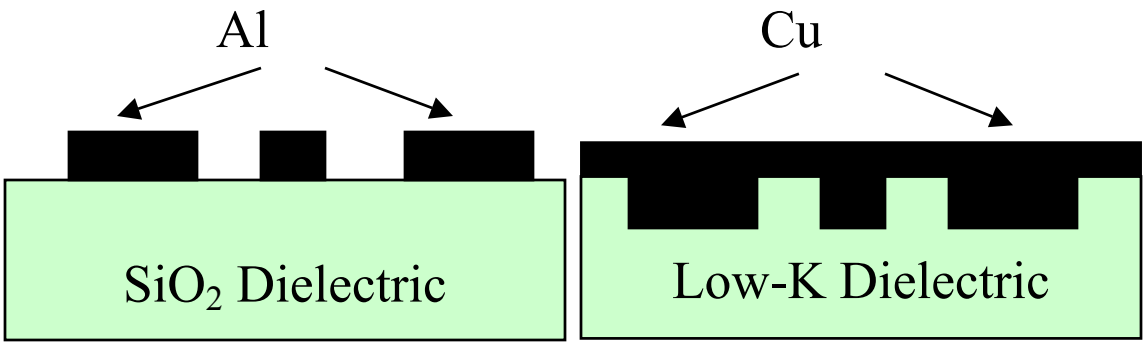


Figure 1. Schematics of Al/SiO_2 vs. Cu/Low-K processing.

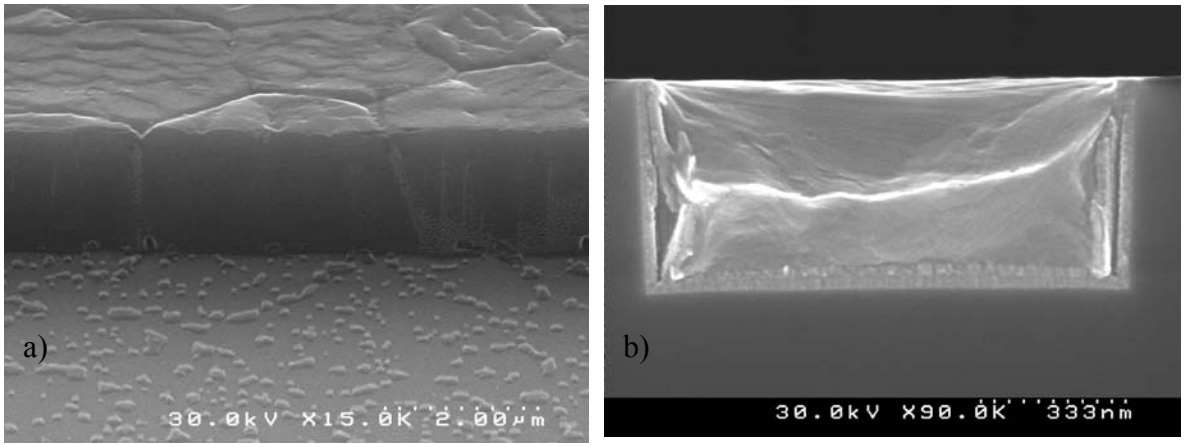


Figure 2. a) SEM side view of an Al line on top of SiO_2; b) SEM cross-section of a Cu line surrounded by a low-K dielectric.

Along with the advanced Cu interconnects, new Low-K dielectric constant materials development is underway. Introducing porosity into the SiO_2 matrix is one of the ways to lower the dielectric constant. Those are typically spin coated organic filled glasses. The pore size is on the order of several nanometers, and pore introduction compromises mechanical properties of low-K thin films, especially fracture toughness, as these materials are typically brittle. While decreasing dielectric constant, increasing porosity compromises films mechanical reliability. Figure 3 shows how dielectric constant depends on the SiO_2–based low-K material density. While fully dense SiO_2 has a dielectric constant of 4.2, and air has a dielectric constant of 1 by definition, Low-K dielectric constant is determined by the mixture rule (Figure 3). Organo-silicate glass (OSG) is one of the novel low-K interlayer dielectrics (ILD) to replace SiO_2 in modern microelectronic devices. OSG is a nanoporous

material with up to 50% porosity, and an average pore size on the order of nanometers. It is typically deposited by spin coating with a consequent drying step.

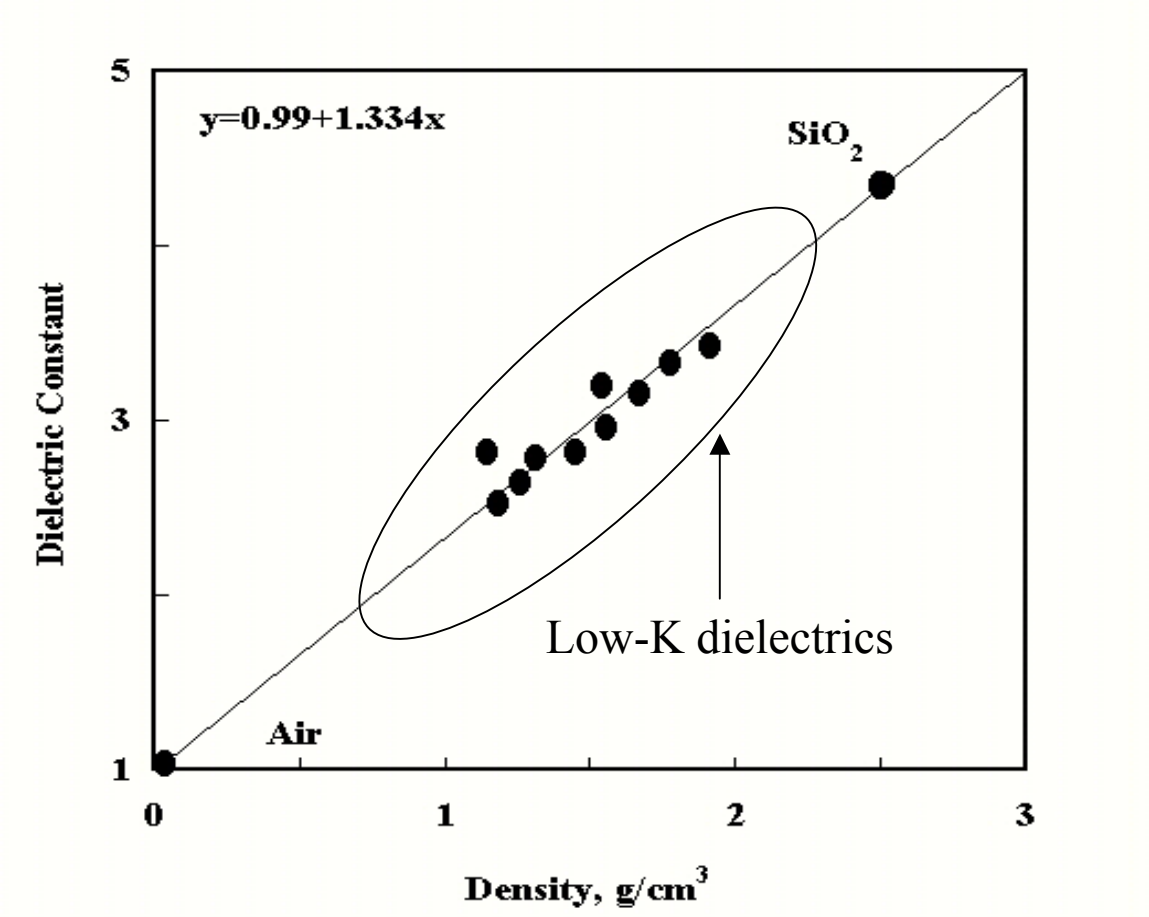


Figure 3. Dielectric constant as a function of low-K density.

Since mechanical properties and interconnect reliability are tightly linked with microstructure, we will describe some characterization techniques as applied for advanced interconnect materials.

Advanced Interconnect Materials Characterization

Microstructure of Cu interconnects (grain size and grain orientation) is likely to be important in determining its reliability, as has been observed in Al based interconnects [3]. The microstructure of Cu as well as the design of the metal stack is fundamentally different as compared to Al-based metallization, since the dual damascene process is used for Cu technology. In the dual damascene process, trenches in the dielectric material are filled with a barrier layer and electroplated Cu. Depending on electroplating conditions and the type of barrier layer, this process results in a large variety of microstructures, mainly small grained and low textured [4-6]. Electroplated Cu is also known to self anneal at room temperature. In order to address issues related to reliability and process improvement, microstructure of Cu was analyzed with respect to processing conditions, such as type and deposition of

the barrier layer, plating conditions, stack geometry (e.g. film thickness) and post electroplating annealing steps [6-9].

Now we will outline major techniques for measuring thin film residual stress, grain size and texture. The average residual biaxial stresses in the films can be calculated from Stoney's equation by means of the wafer curvature technique:

$$\sigma_R = \frac{E_s}{1-\nu_s}\frac{h_s^2}{6h_f R} \quad (1),$$

where E_s is the substrate elastic modulus, and ν_s is the substrate Poisson's ratio, h_s is the substrate thickness, h_f is the film thickness, and R is the substrate radius of curvature. Thin film elastic modulus is not required for this method. Typical test accuracy is within a 50 MPa range. Stresses in thin films may vary by 50% throughout the wafer (Figure 4). Usually the film stress is not isotropic, and the substrate curvature varies in different directions, so equation 1 takes the following form:

$$\sigma_R = \frac{E_s}{1-\nu_s}\frac{h_s^2}{6h_f R_1}\cdot\left[1+\left[\frac{\nu}{1+\nu}\right]\cdot\left[\frac{R_1}{R_2}-1\right]\right] \quad (2),$$

where R_1 and R_2 are the radii of curvature in the x-z and y-z planes respectively. Substrate curvature radii can be measured accurately with laser deflection and optical lever cantilever beam techniques. This allows constructing a stress map over the whole wafer (Figure 4), although this is still a macroscopic average residual stress that is calculated. Wafer-level film residual stress maps can be obtained using FSM 128 stress measurement system [10]. FSM 128 performs 12 scans of the surface of a wafer before and after film deposition. Local stress is calculated employing equation 2. Similar to continuous films, this technique can also be used for arrays of parallel interconnect lines, although X-Ray diffraction techniques are better suited for lines. Measuring residual stress as a function of temperature also provides additional information about interconnects behavior [8, 11].

It is important to measure thin film grain size, since it affects the mechanical properties, specifically yield stress. In the case of a nanocrystalline columnar grain Cu film its grain size can be measured by means of Atomic Force Microscopy (AFM), where grains can be resolved on the surface. Measurements from the AFM section analysis provide the average grain size. One of the problem with electroplated Cu films grain size measurements is that annealing causes grain coalescence through the film thickness, but not necessarily surface reconstruction that would replicate the new bigger grain size. Focused Ion Beam machining (FIB) is a more suitable technique for the thin film grain size measurement. It is similar to the Scanning Electron Microscopy (SEM), except instead of the electron beam, a focused ion beam of Ga is used to raster along the sample surface. FIB can also be used to clean the surface from an oxide by sputtering the film material away. The image is constructed by collecting secondary ions or electrons, which produce a contrast according to the grain orientation. FIB image of a 2 μm thick electroplated Cu films are presented in Figure 5. The sample is tilted 45° to the ion beam, so all grains appear elongated in the horizontal direction. Grain size can be directly measured from Figure 5, where intragranular contrast is due to Cu twinning. While more time consuming, TEM can also be used for grain size measurements.

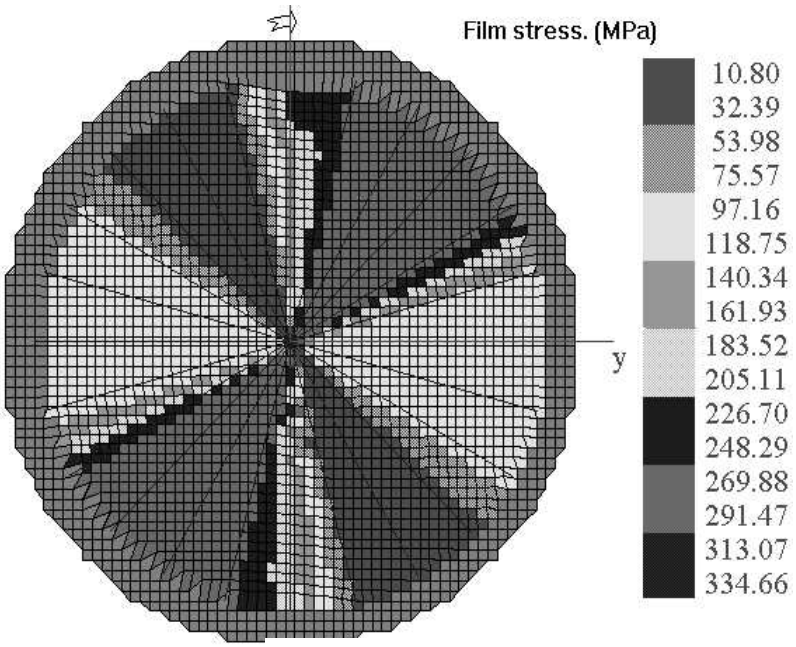


Figure 4. Wafer stress map of a 2 μm annealed Cu film.

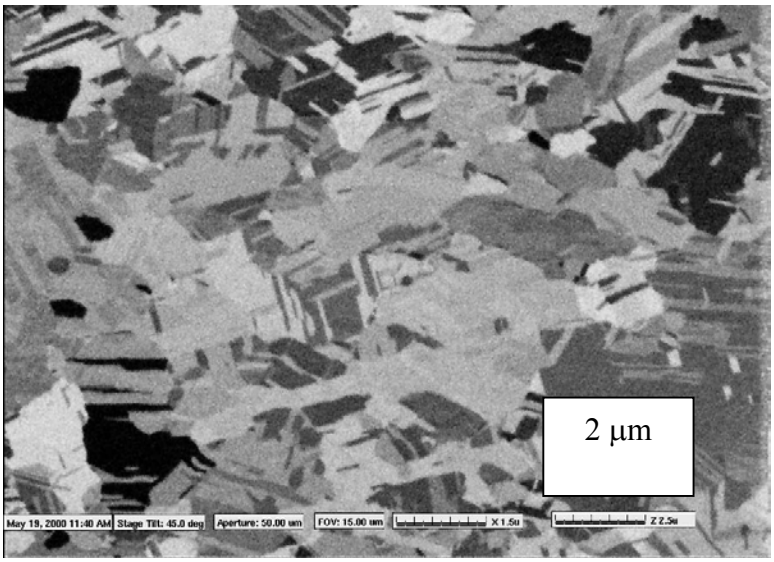


Figure 5. Focused Ion Beam image of a 2 μm thick electroplated Cu film (45° tilt).

Typically electroplated Cu films have (111) texture. When the residual stress and the mechanical properties of various Cu films are very similar, X-ray pole figure analysis technique can show the difference in electroplated Cu films properties on different underlayers in terms of their microstructure. Figure 6 shows a (111) pole figure obtained from a horizontal array of Cu interconnect lines on top of a TaN underlayer. Pole figure shows standard (111) peak intensities at 0 and 70.5°, as well as (511) twins. Vertical features are the (111) intensities from the interconnect sidewalls.

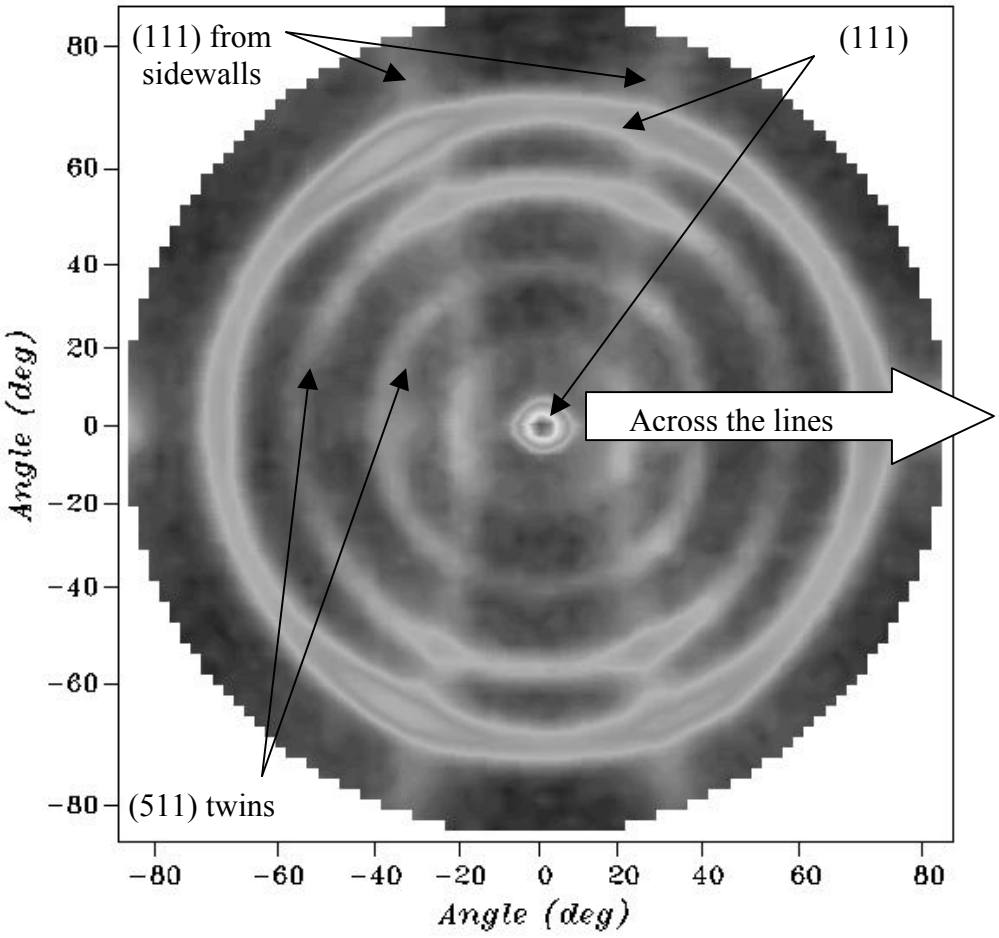


Figure 6. (111) pole figure of a 500x500 μm parallel Cu lines array on TaN underlayer.

X-Ray techniques can also be used for characterizing low-K dielectrics. We have attempted to measure low-K film density using X-Ray reflectivity (Figure 7) [12]. The best fit was obtained by using a thin intermediate SiO_2 layer, and the fitting parameters are shown in Figure 7 [13]. The thickness measurement of 820 Å was confirmed with spectroscopic ellipsometry, and the 50% density of SiO_2 was confirmed with RBS measurements [12]. Pore size distribution greatly affects low-K dielectric properties. Porosity can be measured by cross-sectional TEM [14], small angle X-Ray scattering [15], or by spectroscopic ellipsometry combined with nanoindentation [16, 17]. The effects of pore size on the mechanical properties are considered in [12]. At this point we will discuss nanoindentation techniques for measuring thin film mechanical properties.

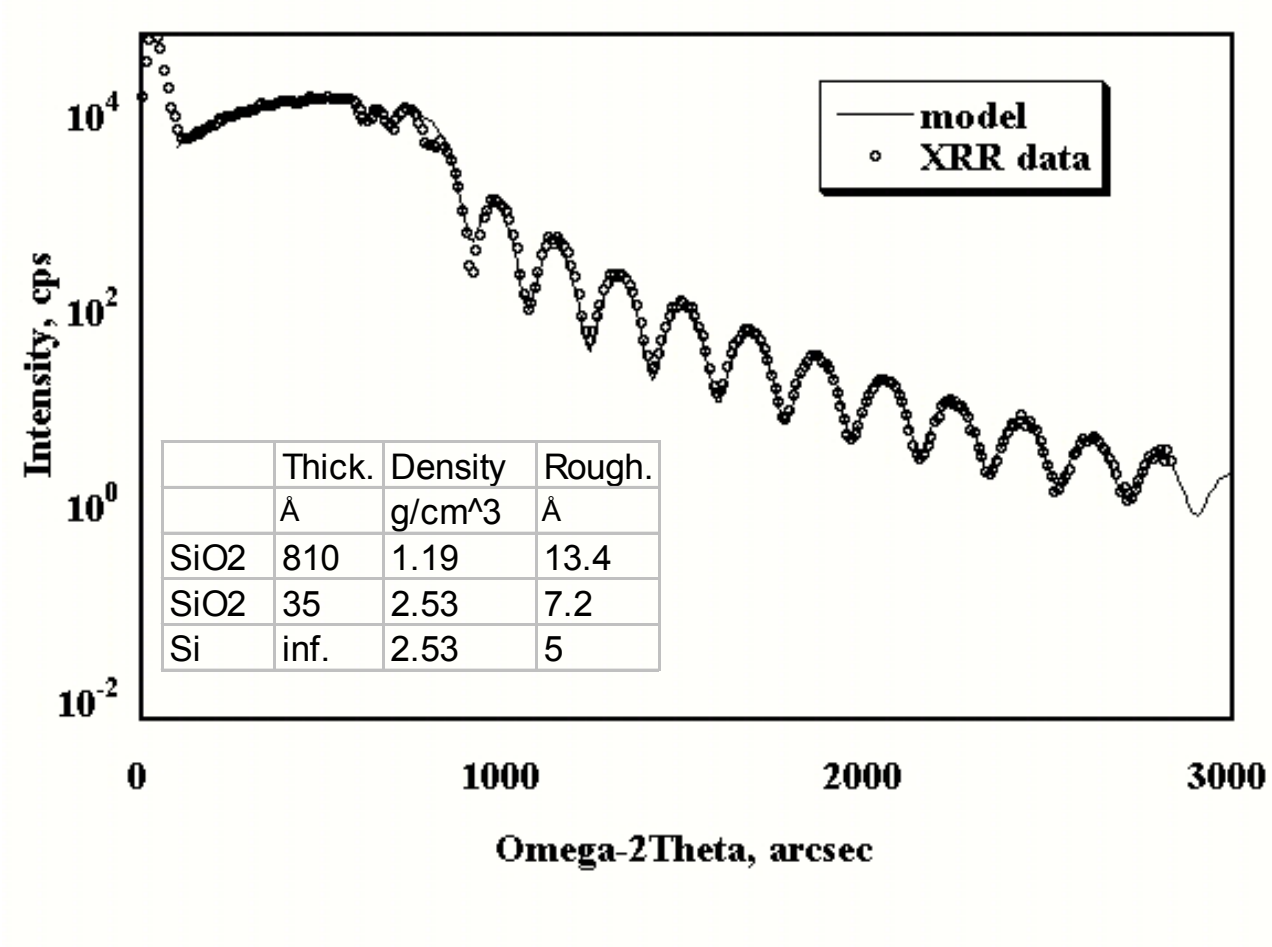


Figure 7. X-Ray reflectivity data along with a model fit obtained from an 80 nm thick low-K film.

Elastic Modulus and Hardness

Thin film mechanical properties (elastic modulus and yield strength) can be measured by tensile testing of freestanding films [18] and by the microbeam cantilever deflection technique [19, 20]. Nanoindentation is an easier way, as no complicated sample preparation is required and tests can be performed quickly and inexpensively. Nanoindentation is similar to conventional hardness tests, but is performed on a much smaller scale using special equipment. The force required to press a sharp diamond indenter into tested material is recorded as a function of indentation depth. Both elastic modulus and hardness can be readily extracted directly from the nanoindentation curve [21-24]. Since the depth resolution is on the order of nanometers, it is possible to indent even very thin (< 100 nm) films. A typical load-displacement curve of a 1 μm thick Cu film is shown in Figure 8.

Elastic modulus is determined based on the knowledge of the tip shape function, A and the load-displacement curve (load *P* and displacement *h*) [22]:

$$E_r = \frac{\sqrt{\pi}}{2}\frac{dP}{dh}\frac{1}{\sqrt{A}} \qquad (3).$$

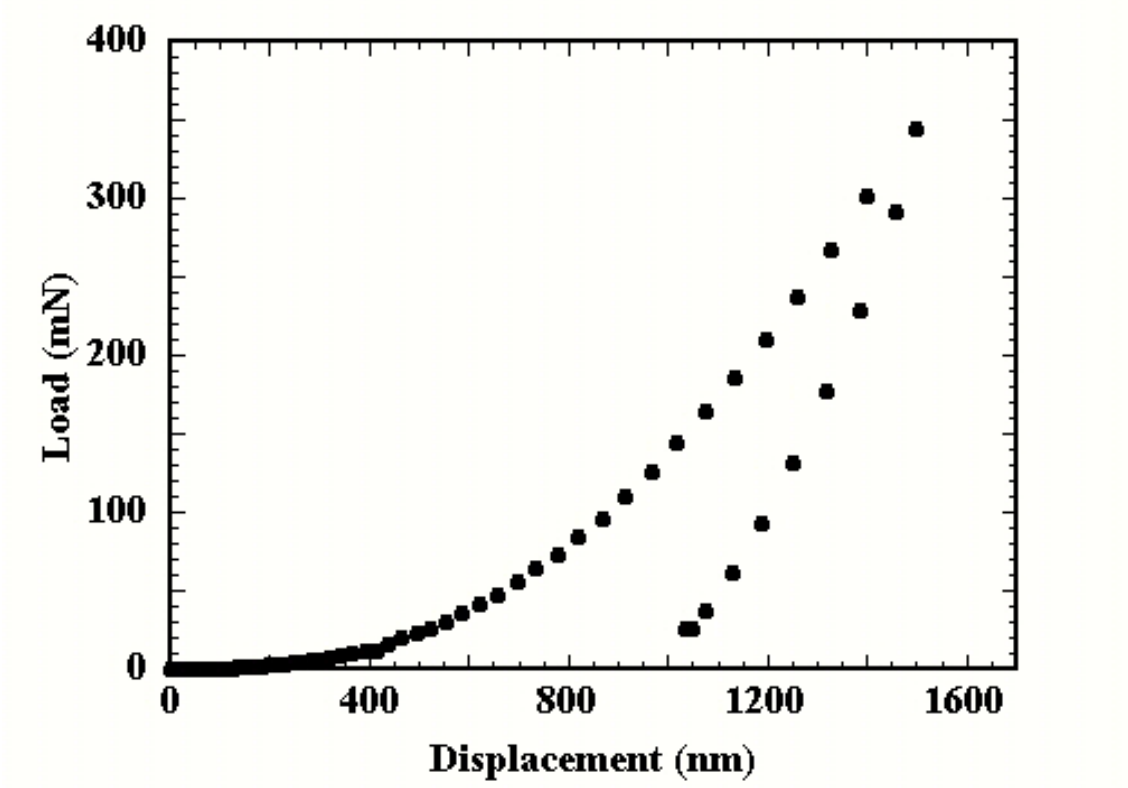


Figure 8. Load-displacement curve for a 1 μm thick Cu film.

Here, $\frac{dP}{dh}$ is taken for the unloading portion of the curve (Figure 8), and E_r is the reduced modulus:

$$\frac{1}{E_r} = \frac{1-\nu_1^2}{E_1} + \frac{1-\nu_2^2}{E_2} \quad (4),$$

where ν_1 and ν_2, E_1 and E_2 are Poisson's ratios and elastic moduli of the film and the indenter material respectively. Hardness is defined as the ratio of indentation load and projected contact area:

$$H = \frac{P_{\max}}{A_{projected}} \quad (5).$$

For a metal film the yield stress, σ_{ys}, can be taken as 1/3 of the hardness [25] measured by nanoindentation, or more accurately it can be extracted from the extent of the plastic zone size around the indenter, c, measured by AFM, using Johnson's spherical cavity model approach [26, 27]:

$$\sigma_{YS} = \frac{3P_{\max}}{2\pi c^2} \quad (6),$$

where P_{max} is the maximum indentation load. Although this was originally applied for the bulk materials, it was also shown to be applicable in the case of thin films [7].

In the case of a metal thin film, the yield stress is typically much higher than for a bulk material. Since metal films are typically nanocrystalline, this is explained by the Hall-Petch type relationship between film yield stress and its grain size, *d*:

$$\sigma_{YS} = \sigma_i + kd^{-n} \tag{7},$$

where σ_i is some intrinsic stress, independent of the grain size *d*, and *n* is typically between 0.5 and 1. The classic $1/d^{0.5}$ Hall-Petch relationship is not typically observed for thin films due to the substrate effect, limiting thin film plasticity, or due to the dislocation looping along the metal/oxide interface [28]. Similar effects are observed in different nanocrystalline bulk materials and thin films [29, 30]. This should not be confused however with the bulk material surface preparation effects on the hardness [31].
If the grain size of a thin film scales with the film thickness, *t*, the film thickness can be used instead of the grain size as a scaling parameter [32]:

$$\sigma_{YS} = \alpha\left(1 + \beta t^{-1/2}\right) \tag{8},$$

where α and β are the fitting parameters. A similar approach, based on the film thickness is used by Nix [28] to predict Cu flow stress behavior.

Electroplated Cu grain size was obtained using both AFM and Focused Ion Beam (FIB) imaging, as described in the previous section, and the yield stress was measured by nanoindentation, taking 1/3 of the hardness and also using equation 6 [7]. For electroplated annealed Cu films the following dependences of yield stress (in MPa) on grain size and the film thickness can be used:

$$\sigma_{YS} = 180 + 0.262d^{-1/2} \quad \text{or} \quad \sigma_{YS} = 230 \cdot \left(1 + 0.577 \cdot t^{-1/2}\right) \tag{9},$$

where *d* is the thin film grain size in microns, and *t* is the film thickness in microns.

As grain growth is typically observed in electroplated Cu films at room temperature (self-anneal process), thermal treatment is necessary, and may drastically affect thin film performance through altering microstructure. This includes both electromigration performance and the change in plasticity properties as depicted by equation 9. Cu films plastic properties strongly depend on the ambient temperature [33]. Plasticity of metal films greatly affects their adhesion performance as will be discussed in the next section.

Elastic modulus and hardness of different low-k materials were previously measured using nanoindentation [14, 17, 34, 35], depending on the amount of porosity and composition, the elastic modulus of low-K dielectric films varied from 2 to 14 GPa, and the hardness varied from 0.5 to 2 GPa. A linear relationship between the elastic modulus and hardness was found for the silicate low-K dielectric films when using Oliver and Phar analysis or Continuous Stiffness Measurement (CSM) approach with sharp Berkovich indenters [14, 34, 35]. As the mechanical response of low-K dielectric films is quite different from metallic films, in a way that the former exhibit almost no plasticity (Figure 9) [12], it may be appropriate to use Hertzian analysis with blunter spherical tips for extracting elastic properties. For elastic Hertzian contact indentation load is related to indentation depth as:

$$P = \frac{4}{3} E_r \sqrt{Rh^3} \tag{10}.$$

Now the reduced film modulus can be readily extracted from equation 10 if the spherical tip radius, *R* is known and the loading and unloading curves are elastic as in Figure 9 [9, 12]. Another possibility would be to use a thin passivation layer on top of the low-K film in order to avoid surface effects.

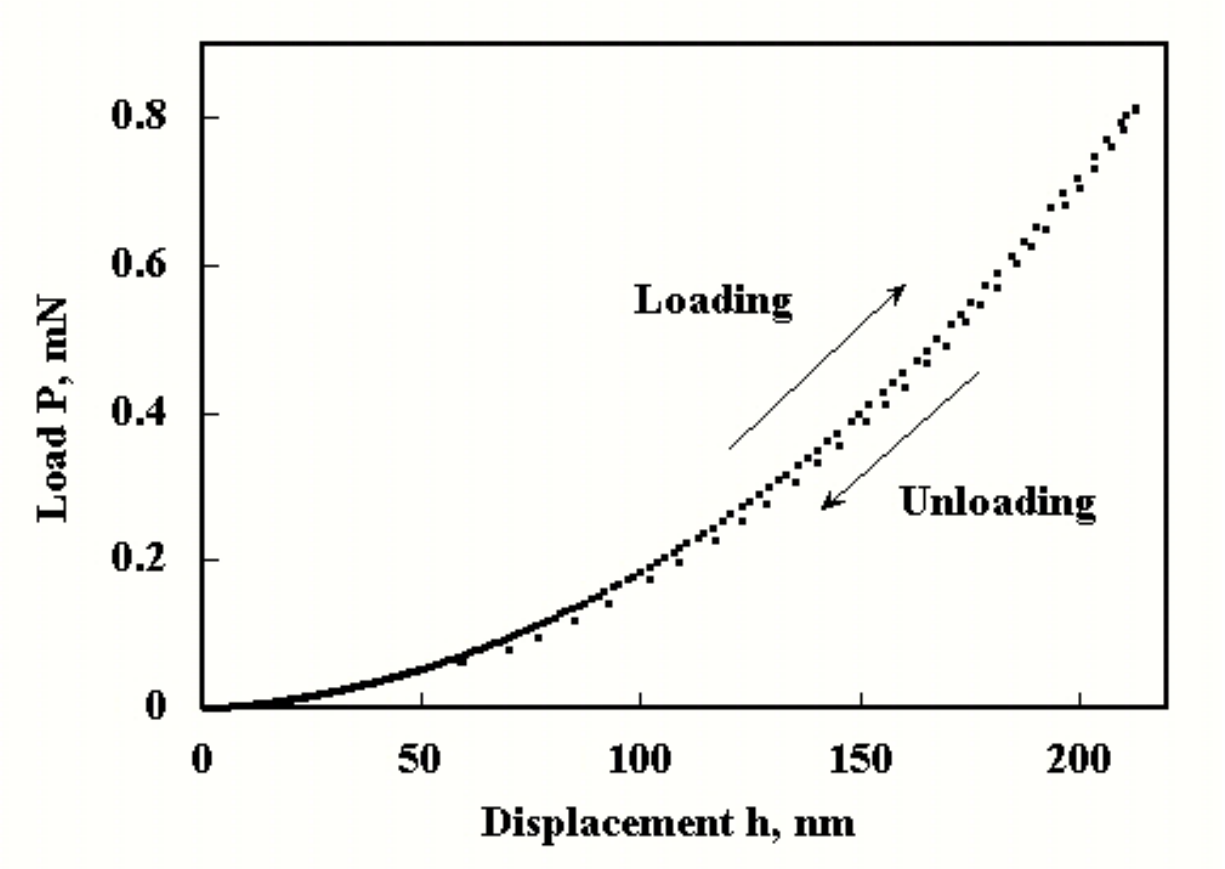


Figure 9. Load-displacement curve for a 1 μm thick low-K film.

Adhesion and Fracture Toughness Measurements

Indentation has been also used to measure thin film adhesion [36-40], where the mechanical energy release rate, or practical work of adhesion is calculated based on the size of delamination that can be generated by high load (200-800mN) indentation. For the most well adhered and ductile films a highly stressed superlayer needs to be deposited on top of the tested film. Deposition of a hard film, capable of storing sufficient amounts of elastic energy over the film of interest, can result in multilayer debonding [41], producing larger delamination radii. It also acts like a capping layer, preventing plastic flow of the underlying film in the vertical direction, adding normal stresses at the interfacial crack tip [37-39]. For the superlayer indentation test a sharp indenter also provides additional stress for crack initiation/propagation at the interface. A superlayer test schematic is presented in Figure 10. There would always be a plastic zone size around the indenter, and, depending on the testing material, ahead of the interfacial crack tip. It is important to make sure that those plastic zones do not overlap. Typically, the delamination radius has to be at least three to five times larger than the indenter contact radius in order to avoid this phenomena, also called the tip interaction effect [39]. The practical work of adhesion is calculated based on the Marshall and Evans analysis [36]:

$$\frac{GE_f}{(1-\nu_f)} = \frac{1}{2} t\sigma_I^2(1+\nu_f) + (1-\alpha)(t\sigma_R^2) - (1-\alpha)t(\sigma_I - \sigma_B)^2 \quad (11),$$

where E_f and ν_f are the thin film's Young's modulus and Poisson ratio respectively, t is the film thickness, σ_R is the residual stress in the film, σ_I is the indentation stress from the indenter, σ_B is the Euler buckling stress of the film stack. The term α is equal to one if the film is not buckled, otherwise it represents the slope of the buckling load versus the edge displacement on buckling: $\alpha = 1 - \frac{1}{1 + 0.902(1-\nu_f)}$. Kriese and Gerebrich have modified this analysis and employed the laminate theory in order to calculate the necessary terms in equation 11 for the bilayer [37]. In the case of a highly compressed superlayer, the indentation stress is being added to the residual stress, so multiple superlayer depositions are avoided. Blanket films can be tested in the as-deposited, as-processed conditions; no pattern transfer is necessary. When an indenter penetrates through a bilayer, it causes film debonding and blister formation, which can be seen afterwards in an optical microscope with Nomarski contrast (Figure 11).

Properties of thin films such as elastic modulus, Poisson's ratio, as well as the tip angle and radius are needed for an adhesion assessment. Two measurements are necessary for strain energy release rate calculations. From the standpoint of blister formation, indentation depth, h, and blister diameter, a, are required. Blister diameter is measured in the optical microscope with Nomarski contrast. Using the Oliver-Pharr method [24], inelastic indentation depth, h_{pl}, is calculated from:

$$P = \alpha\left(h - h_{pl}\right)^{\beta} \quad (12),$$

where P and h are the load and displacement from the 65% of the unloading slope of the load-displacement curve respectively, α and β are fitting parameters. The indentation volume, V_I, is calculated from inelastic depth by using the tip geometry. The indentation stress can be calculated as in [24]:

$$\sigma_I = \frac{V_I E_f}{2\pi t a^2 (1-\nu_f)} \quad (13),$$

assuming the volume conservation.

Figure 12 shows the practical work of adhesion for a Cu film as a function of film thickness. The data presented is for Cu films deposited on SiO_2 and Ti layers on top of Si. As previously discussed in [26-31], there is a plastic energy contribution to the practical work of adhesion that increases with the film thickness over a 100 nm. Below a 100 nm film thickness almost no plasticity effects are observed, and the measured work of adhesion is approaching the thermodynamic work of adhesion of 0.6 and 4 J/m^2 for the Cu/SiO_2 and Cu/Ti interfaces respectively.

A simple plastic strip model [38] can be used as an upper bound for predicting practical work of adhesion of a metal thin film:

$$G \approx t\frac{\sigma_{YS}^2}{E}\left\{\ln\left[\frac{t}{b}\right] - 1\right\} \quad (14),$$

where t is the film thickness, and b is the burgers vector. More advanced models can be found in [38, 39, 42].

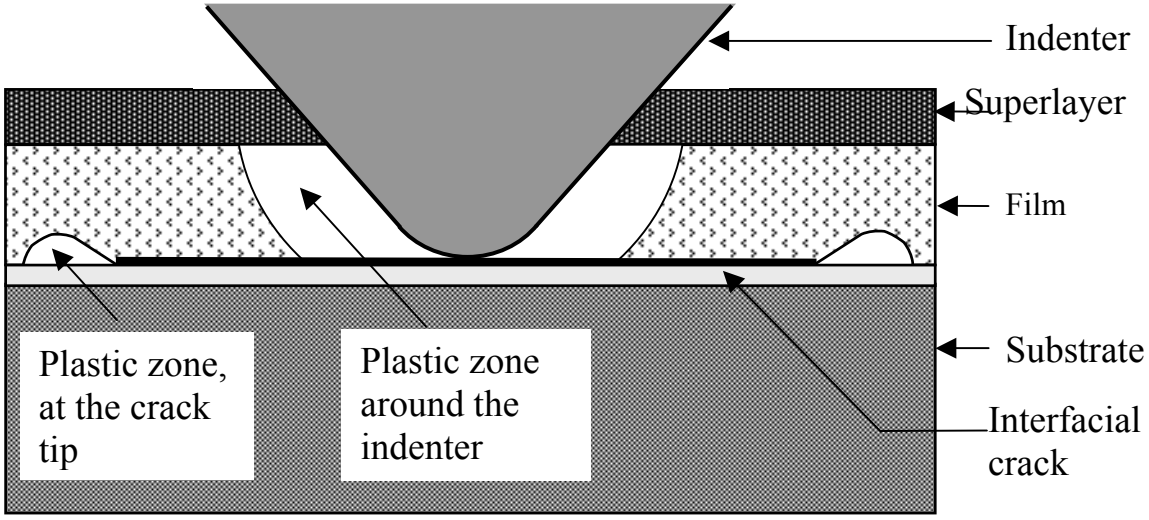


Figure 10. Schematic of the superlayer indentation test (After figure 2 in [38]).

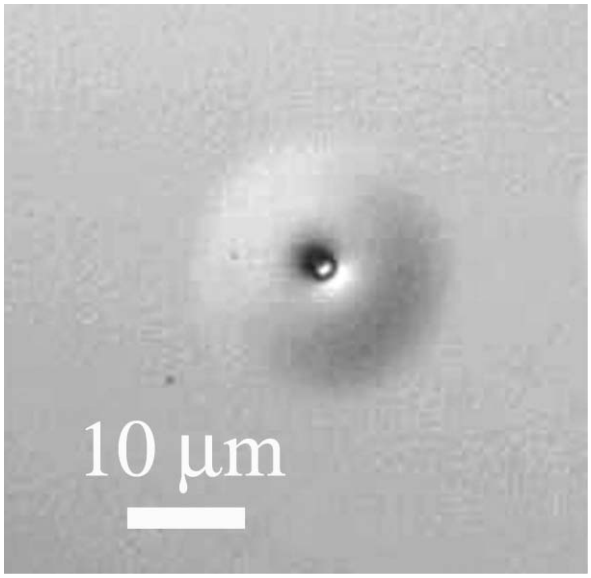


Figure 11. Nomarski contrast optical image of a W/Cu film stack delamination.

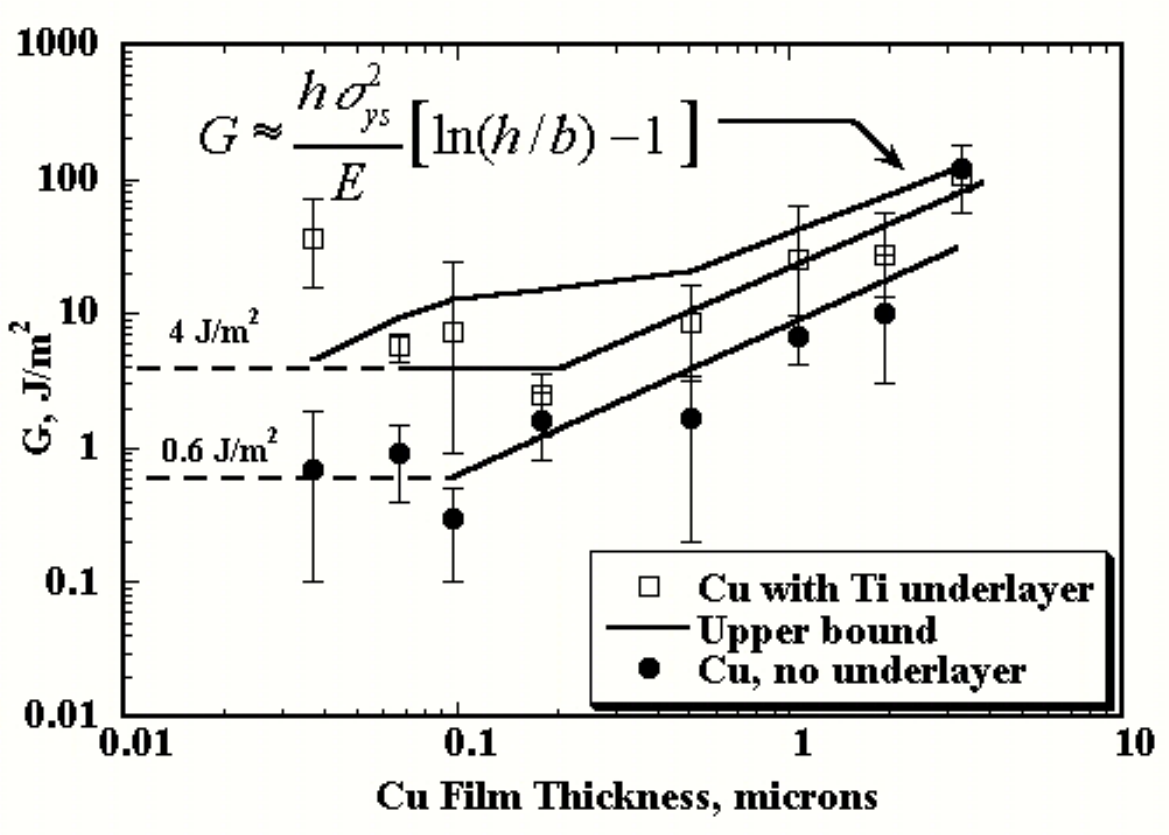


Figure 12. Cu film practical work of adhesion as a function of film thickness (after Figure 8 in [38]).

Attempts have been made to measure the adhesion of low-K dielectric films to various substrates [14, 35], and varied from 0.1 to 4.5 J/m^2. However, ex-situ FIB cross-sectioning of the delamination blisters showed that in most cases fracture occurred in the low-K dielectric layer itself [14]. This phenomenon occurs since the interfacial fracture toughness (or adhesion) of the low-K/substrate interface exceeds the fracture toughness of the low-K material itself [14, 35]. Fracture toughness is an important property to measure for the low-K dielectrics along with the interfacial adhesion.

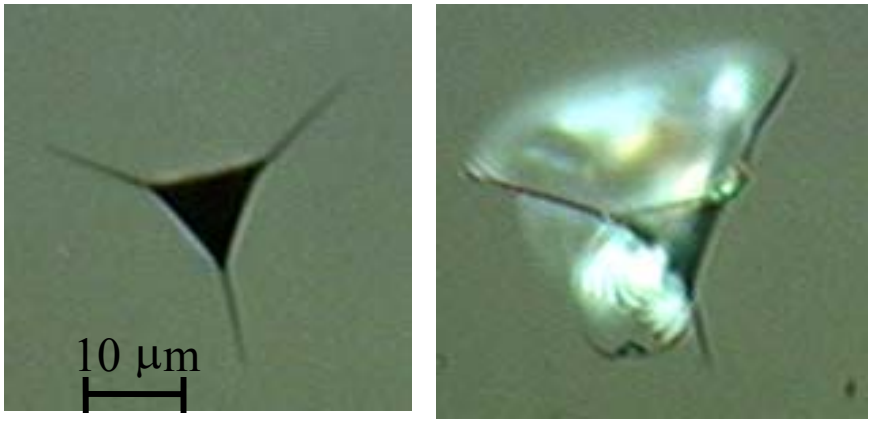
Fracture toughness of a bulk brittle material can be calculated within 40% accuracy based on the maximum indentation depth, P_{max} and the crack length, a [43, 44]:

$$K_C = \beta\left(\frac{E}{H}\right)^{1/2}\left(\frac{P_{\max}}{a^{3/2}}\right) \tag{15}$$

where β is an empirical constant which depends on the geometry of the indenter, and is 0.0319 for a cube corner indenter geometry [43, 44], E is the elastic modulus, and H is the mean hardness. Although, technically speaking, any type of pyramid can induce radial cracks, it was shown that the cube-corner indenter provides a lower cracking threshold in terms of the maximum indentation load [44].

Figure 13 represents different scenarios one may observe using pyramid indentation. Figure 13a is the desired configuration for radial cracks emanating from the corners of an indent. Due to the high shear stresses induced by the indenter pyramid edges subsurface delamination cracks are also observed

for some indents (Figure 13b). Similar fracture patterns have been observed in low-K films [14]. Lawn and Wilshaw [45] provide a detailed review of the indentation-induced cracking in brittle materials.



a) b)

Figure 13. Optical micrographs of cube-corner indentation-induced fracture in fused silica: a) Radial cracks; b) Radial and sub-surface cracks.

In theory equation 15 should not be directly applied in the case of a thin film, since typically the crack shape is no longer halfpenny shape. An appropriate model should account for at least the film thickness and stress, and, preferably for the film porosity. Recent theoretical and experimental developments address this problem [14, 17].

For a certain film thickness/load combination there is a linear dependence between the maximum indentation load and the radial crack length to the 1.5 power, $a^{3/2}$ [14]. With certain reservations equation 15 can be used to estimate fracture toughness of thin films (Figure 14). In our previous studies [14, 35] it was found that low-K dielectrics deposited on appropriate barrier layers are susceptible to cohesive, rather than interfacial fracture. Indentation fracture toughness measurements also agreed with the superlayer indentation test results, where cohesive low-K fracture was observed, and with an upper bound estimates based on the fact that some films fractured upon superlayer deposition [14].

Low-K film cracking has also been observed due to the relief of residual stress at a critical film thickness, on the order of 3 μm (Figure 15). This can be used as another method of estimating the film fracture toughness. The low-K dielectric film tensile residual stress is approaching 44 MPa starting from the 0.5 μm film thickness [35], so one can estimate the strain energy release rate, G for this material following Hutchinson and Suo [46] analysis:

$$G = Z\frac{(1-\nu_f^2)\sigma_R^2 t}{E_f} \qquad (16),$$

where σ_R is the residual stress, t is the film thickness, and E_f is the film elastic modulus, and Z is ranging from ½ to 4, depending on the sample geometry and the residual stress sign. In the case of 44 MPa tensile residual stress (Z=1/2) for a 3 μm critical film thickness, one would get 0.581 J/m^2 energy release rate, corresponding to about 0.054 MPa·m$^{1/2}$. A simple analysis like this can provide realistic upper estimates of the thin film adhesion/toughness.

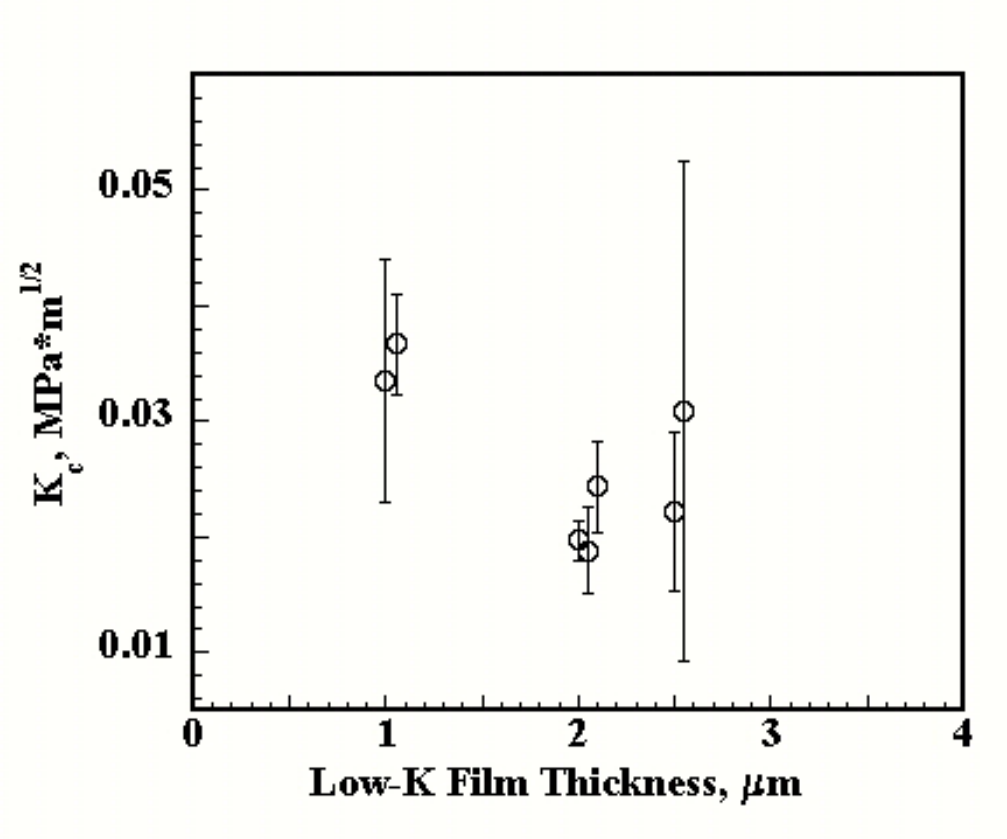


Figure 14. Low-k film fracture toughness.

Based on the knowledge of the residual stress and the film thickness, one can come up with a fracture criterion just due to the residual stress [14]:

$$K_C \le \sigma_R \sqrt{Zt} \qquad (17).$$

Equation 17 is similar to a definition of *K*, except here the film thickness is used instead of the flaw size, or the crack length [47].

It is also important to remember that most of the mechanical properties change with temperature. With certain hardware modifications nanoindentation can be suited for measurements at higher temperatures, which is currently being investigated.

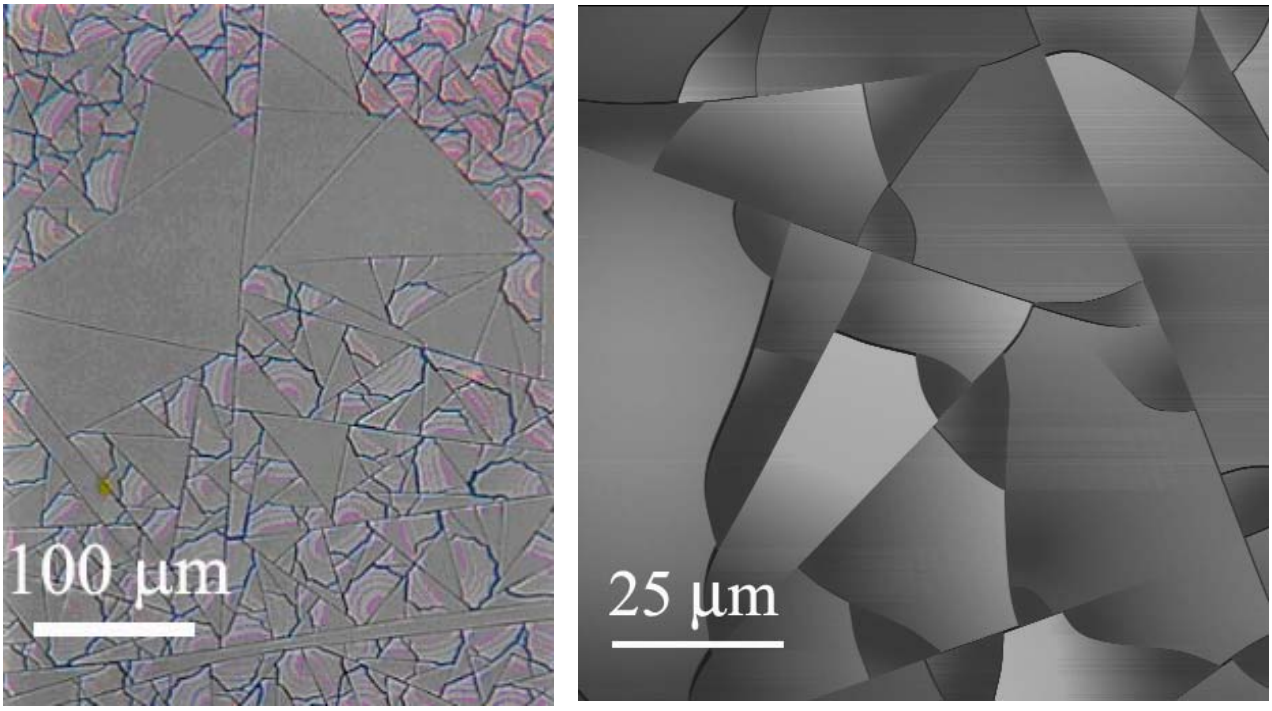


Figure 15. Optical and AFM images (1 μm Z range) of a 3 μm thick low-K film cracking due to residual stress relief (after Figure 12 in [9]).

Conclusions

Nanoindentation is a powerful technique that can be applied in modern microelectronics for measuring thin film mechanical properties. While measuring elastic and plastic properties with nanoindentation is almost routine, and there are several commercial tools and software packages available, adhesion and fracture toughness measurements are still in the development stage. They require support of other characterization techniques, but can be adapted for production quality control applications.

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