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# FIB failure analysis of memory arrays

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**Abstract**

Many modern microelectronic chips contain embedded memory arrays. A typical memory bit-cell contains several transistors. Failure of a single transistor or contact within a bit cell makes the entire bit cell inoperable. A dual-beam Focused Ion Beam (FIB) tool combines milling capability with in situ Scanning Electron Microscope (SEM) imaging, which is very useful for identifying the root cause when a physical defect is present. This paper describes the slice-and-view FIB technique for failure analysis (FA) in memory arrays. Several failure mechanisms have been identified, including missing patterns, killer particle defects, shorted and open stack vias. Transmission Electron Microscopy (TEM)/Scanning TEM (STEM) analysis was able to provide additional information when SEM resolution was not sufficient. Processes were adjusted appropriately leading to yield enhancement.


## 1. Introduction

In 1965, Gordon Moore [1] observed exponential growth in the number of transistors in integrated circuits, and predicted that the trend would continue. According to Moore's law the number of transistors in a microprocessor chip doubles every couple of years. The microelectronics industry has been keeping up with this pace by advancing technology and reducing feature sizes, in accordance with the International Technology Roadmap for Semiconductors (ITRS). The ITRS is an assessment of the semiconductor technology requirements, based on input from global industry manufacturers and suppliers, government organizations, consortia, and universities to ensure the advancement of integrated circuit performance [2]. One example of this technological advancement is the industry transition from $Al/SiO_2$ to Cu/low-K dielectrics, which started about five years ago.

Some of Motorola's chips have both logic and memory cache arrays, including Static Random Access Memory (SRAM) integrated into one chip for better performance. Millions of transistors are allocated for integrated memory arrays, and are very sensitive to process variation. Therefore

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memory arrays are frequently used as a qualification vehicle for process development. As a result, failure analysis of memory arrays is critical not only for trouble-shooting and problem-solving, but also for assurance of on-time delivery of products to market.

A typical bit cell contains of 4–8 transistors (Fig. 1). If just one out of millions of transistors is not working properly, a part or the whole of the chip becomes inoperable. During manufacturing, certain types of defects can be identified by in-line metrology, and others cannot. Integrated memory arrays can only be fully tested when the entire device is completed. That is why post-production characterization and failure analysis become extremely important, particularly for memory arrays in integrated circuits. At the same time, due to reduced feature sizes, characterization techniques have to meet certain high-performance requirements. For example, the magnification and resolution have to be high enough to enable observing a physical defect in a Scanning Electron Microscope (SEM). In some cases the SEM is not capable of resolving the defect, and TEM needs to be employed. Locating defect coordinates on a chip can be a challenge. The absolute memory address of a failed bit is typically available from electrical testing. However, this address needs to be translated into a physical address on the chip ($x$ and $y$ coordinates) for defect analysis and root cause identification. This paper describes the Focused Ion Beam (FIB) milling technique as applied for failure analysis of memory arrays of integrated circuits.

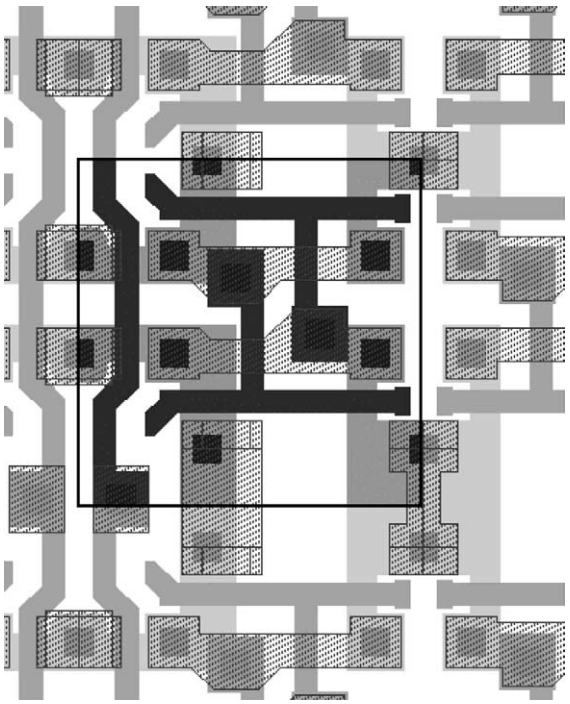

Fig. 1. Schematic of a bit cell containing six transistors.

## 2. Methodology

### 2.1. Sample preparation

In the case of a single, double or a small cluster bit failure, the physical defect is buried under several layers of interconnects. While the defect is sometimes large enough to be visible in the optical microscope (Fig. 2), in most cases it is located below the first metal layer and is not visible. In such cases, the passivation and metal overlayers have to be polished off for failure site identification. An analyst without adequate defect-coordinate information is set up for failure, just as in the case of a person trying to find a house without its address, but using only a large scale country map. The analyst needs the wafer map and the chip layout, as well as the results of the memory test programs. Memory translators capable of con-

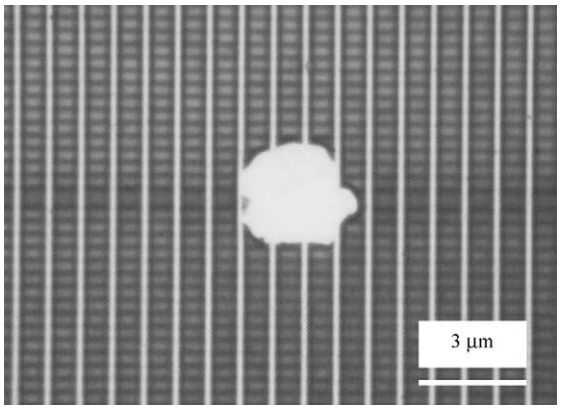


Fig. 2. An optical image of a cluster defect (particle) magnified by the upper layers.

verting an electrical bit address into a physical location on the die can come in handy.

First, bit-cell layouts, at different layers, are studied carefully using CAD software in order to identify appropriate counting and de-processing procedures. For example, the bit cell presented in Fig. 1 has to be de-processed down to the third metal-layer before the stack vias linking two bit cells are exposed.

The correct die is identified, and then cleaved out of the wafer. De-processing is performed by means of polishing the die with a cloth and sub-micron particle slurry, with intervening optical inspections. After polishing, the approximate failure site can be scribed or laser marked for easier site location in the FIB. Without such marking, site identification can be impossible, especially when interconnects are covered with passivation layers. If the sample tends to charge in the FIB, a thin metal coating is required. Regular SEM sample coaters can be used for this purpose.

### 2.2. FIB FA technique

The FIB tool can mill material with a lateral accuracy on the order of 0.1 μm. FIB is also capable of depositing materials. Such deposition is extensively used for circuit modification applications. FIB milling is achieved by focusing a beam of accelerated gallium ions on a specific wafer-site. Any exposed material is milled off by the Ga ion-beam. The FIB is used for site-specific cross-sectioning, interfacial microstructure characterization, preferential removal of specific materials, circuit modifications, TEM sample preparation, and grain imaging.

Dual-beam FIBs are equipped with both ion and electron beams, allowing collection of a secondary electron image, from a specific site, in-between milling cycles [3]. This is essential for failure analysis of memory arrays. Navigation is typically performed in ion-beam mode, with ion-currents limited to 3000 pA, so that FIB fiducial counting marks can be placed and the sample surface is not substantially damaged. In some cases, where the bit cell is quite large, automatic stage positioning can also be employed, which saves quite a bit of time. A top-down FIB image with fiducial counting marks is shown in Fig. 3. Here, the fiducial marks are placed at 2500X magnification with 50 bit lines in-between the marks. After the failure site is identified, a large ($20 \times 10$ μm) trench is milled at a maximum beam current of 7000 pA in the case of an FEI 835 FIB tool. SEM beam alignment can be achieved using active region features shown in Fig. 4. The actual failure-site milling can be performed at 3000 pA with three transistor pairs in view (Fig. 5), which helps identification of abnormalities by comparison of features across the three devices. SEM imaging is done at 15 kV to avoid charging problems present at lower voltage settings. At 15 kV the interaction volume is on the order of microns in

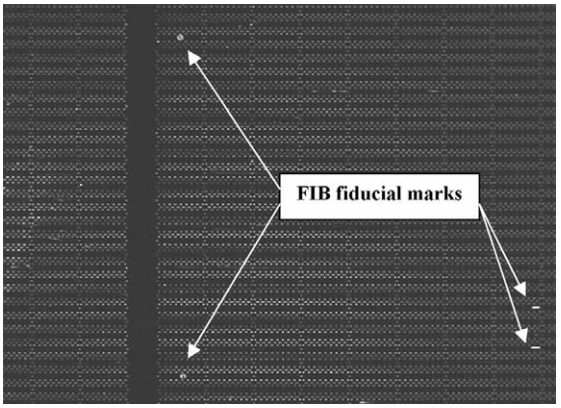


Fig. 3. Top–down FIB image of a memory array showing fiducial counting marks.

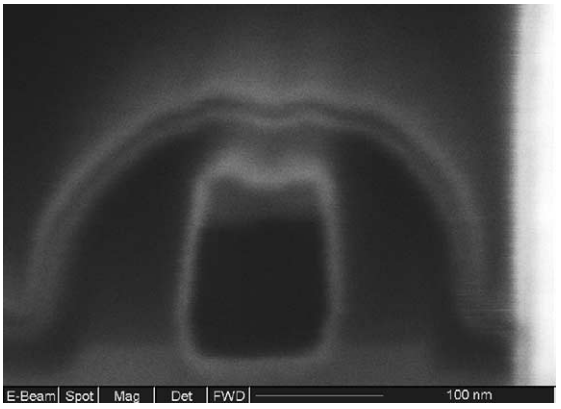


Fig. 4. High-resolution FIB SEM image showing polysilicon spacer.

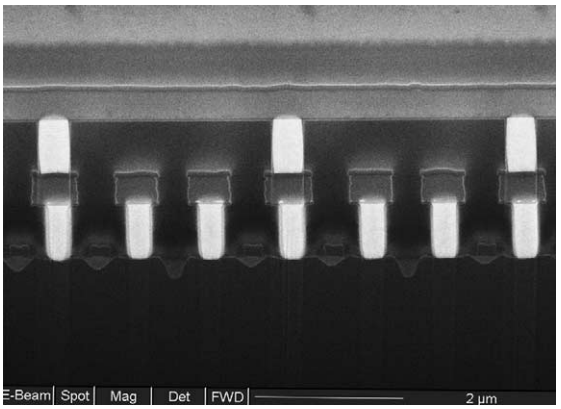


Fig. 5. SEM view of three transistor pairs.

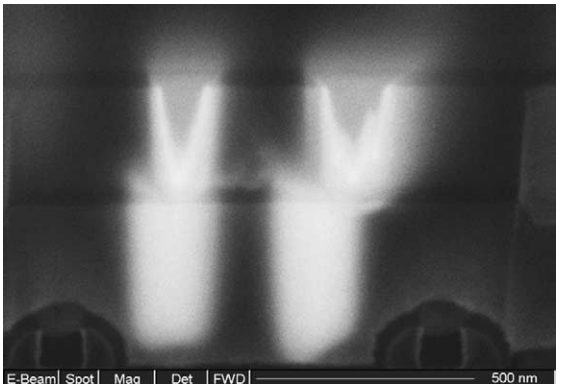


Fig. 6. SEM image showing a defect shadow before milling though it. Here, the FIB cut surface is tilted 38° to the SEM beam, which allows seeing a thin in-plane defect projection.

microelectronic materials, which allows identification of a defect before actually milling through it (Fig. 6). The FIB cut surface is tilted at 38° to the SEM beam. This allows observation of a projection of extremely thin in-plane defects.

The block diagram shown in Fig. 7 represents the entire process of FIB memory-array failure analysis. We will now describe some representative memory array failures and their root causes.

## 3. Failure modes in memory arrays

Several failure mechanisms of memory bits have been reported in literature, including up-shift of threshold voltage and decrease in *trans*-conductance of Ld-PMOS due to local depletion in the poly-Si gate [4], node-to-node and node-to-power-line shorting through CMP scratches [5], electrical opens caused by dangling contacts of the bitline and PMOS [6,7], and bridging of W-plugs through W-extrusion [6]. In all of these cases the feature sizes are on the order of a tenth of a micron or larger.

Given the scaling-down of microelectronics, reduction in the size of devices can increase their sensitivity to process variation. Root causes of failures can be localized to an extremely small size-scale, where SEM resolution is exceeded. We report here failure analyses involving characterization of tiny features down to the size scale of 1 nm using TEM.

Defects that account for most bit failures can be classified as:

1. Killer defects (e.g., particle in Fig. 2),
2. Missing pattern,
3. Incomplete etching, and
4. Shorted or hollow vias.

### 3.1. Killer particles

Killer particles are normally large in size, and along with missing patterns are the root causes of most cluster defects. Particles can be generated by a tool or a process, and are normally recognized by in-line optical metrology. High particle counts are a result of a tool malfunction, and corrective action is required that normally includes temporary process/tool shut down. Particles smaller than 1 μm are usually not detected by means of optical in-line metrology right after they are deposited; instead, they are caught after later processing steps, when the particle size is magnified by subsequently deposited layers, which makes them visible to in-line defect metrology tools. While getting the particles count down is an ongoing effort, particles are unavoidable, and properly implemented defect metrology inspections should keep the problem under control.

### 3.2. Incomplete etching

Fig. 8 is an SEM micrograph obtained in the FIB during a slice-and-view procedure. The image shows via contacts extending from transistor sili-

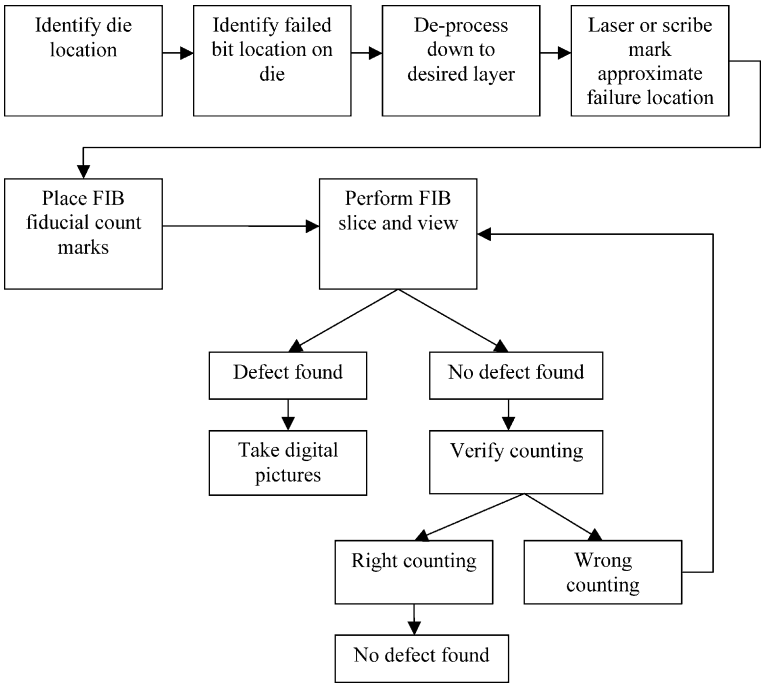


Fig. 7. Block diagram of the FIB failure analysis.

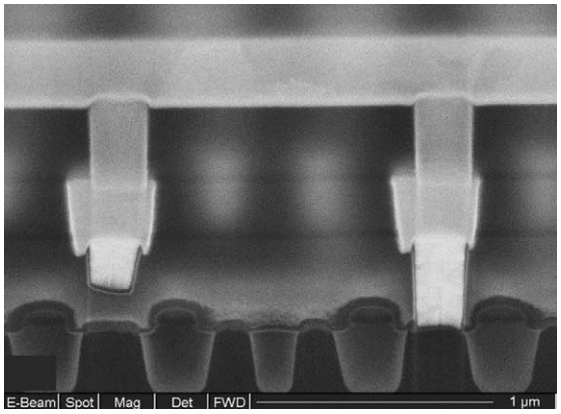


Fig. 8. SEM images of via contacts from transistors to second level metallization. The etch used to create the via on the left was incomplete, resulting in an electrical open.

con to the second level of metallization. The etch step used to create the via on the left was incomplete, resulting in no contact between metal and the transistor. As a result, two adjacent bits are electrically open. The incomplete etching was traced back to a photoresist issue.

### 3.3. Pattern issues

Missing patterns as well as extra patterns also cause bit failures. Fig. 9 shows two electrically opened bits, where the second metal layer is discontinuous above the via between the first and the second metal layers. As an example of metal bridging, another pattern defect is shown in Fig. 10. Here, two second-metal lines are bridged

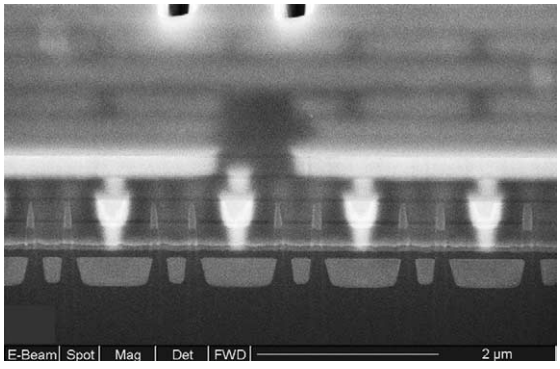


Fig. 9. SEM image of two open bits due to a pattern defect.

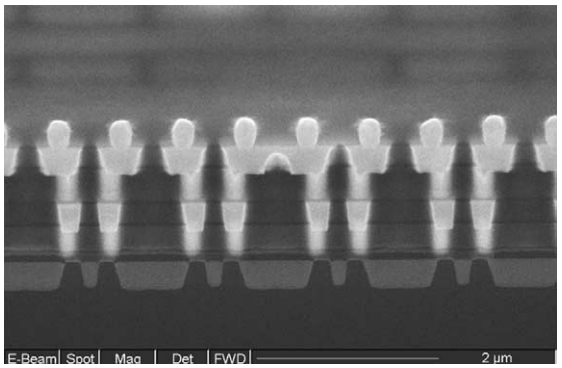


Fig. 10. SEM image of shorted bits. Here, second metal lines in the middle are bridged together.

together. Such bridging was caused by a photoresist issue in patterning of the trenches of the second metal layer, and ultimately led to shorting of the bits.

In some cases determining the failure root cause is not as easy. For example, Fig. 6 shows a defect behind a layer of dielectric. While this defect is seen in the SEM due to a large interaction volume at 15 kV and the fact that the sample is tilted, it is not clear where exactly this defect is located in the stack, and what has caused it to form. TEM analysis along with Energy Dispersive Spectroscopy (EDS) and Parallel Electron Energy Loss Spectroscopy (PEELS) come in handy in identifying the material and the root cause of defects with sub-nanometer resolution.

Brief descriptions of EDS and PEELS are given as follows.

When a probing electron enters a material to be analyzed, inelastic scattering can occur as a result of Coulomb interaction between the incident electron and the atomic electrons. An inner shell atomic electron can absorb an energy that is not smaller than its binding energy and make a transition, allowed quantum-mechanically, to an empty state that is above the Fermi level, leaving the atom in an ionized state. In a subsequent de-excitation process, another atomic electron with a lower binding energy transits into the vacant state (also allowed quantum-mechanically), and the corresponding amount of energy is released as an X-ray photon. Such X-ray photons and inelastically scattered incident electrons carry energies that are characteristic of the constituent elements, and these energies are spectroscopically analyzed in EDS and EELS [8–10].

### 3.4. TEM analysis of shorted and open vias

Fig. 11(a) is a TEM brightfield image of a pair of tungsten plugs in a shorted bit. There is a faint dark layer present between the tungsten plugs. A higher magnification view of the faint layer shown

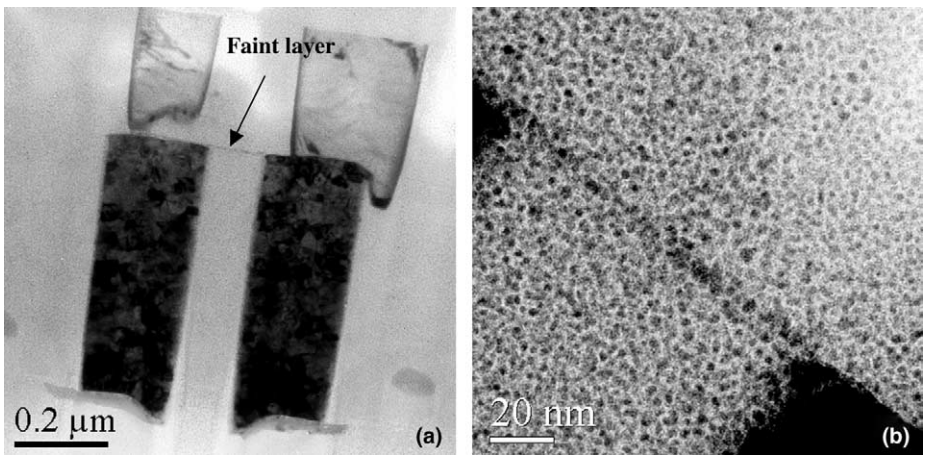


Fig. 11. (a) TEM image of a pair of tungsten plugs in a shorted bit. A faint dark layer between the tungsten plugs is noticeable. (b) A higher magnification view of the faint layer in (a). The dark layer is residual titanium that was left behind by the CMP (chemical–mechanical planarization).

in Fig. 11(b) provides more details. Here, the thickness of the faint layer is measured to be 3–5 nm. Typically, on both sides of FIB-prepared TEM samples, re-deposition and surface amorphization (where applicable) makes resolving fine features like this faint layer difficult in the bright field TEM image [11–13].

In order to identify the material of the layer, EDS–PEELS spectrum imaging was performed, with an electron-probe of a FWHM equal to 1.6 nm. A pair of EDS and PEELS spectra were acquired at each point. The sample was tilted by about 10°, about an axis that is perpendicular to the layer, and towards the EDS detector. This was done to minimize any possibility of the TEM Cu mesh blocking X-rays generated from the sample, while an edge-on view of the faint layer was maintained. EDS and PEELS are complementary techniques in terms of elemental detection efficiency. With the availability of both techniques, elemental analysis becomes more powerful than with either one of them, separately, and especially under circumstances where extremely high-$z$ and low-$z$ elements are present.

An EDS spectrum acquired with the nanoprobe positioned in the middle of the faint layer is shown in Fig. 12(a). Characteristic X-rays of Ti, Si, O, Cu, Pt, Ga and C are present. Among them, the Cu signals are from background generated from the Cu mesh, as well as the Cu in the TEM sample holder. The Si and O signals have contributions from the $SiO_2$ and possibly Si re-deposited on both sides of the TEM sample. The Pt signal is from Pt deposited on the sample at the wafer surface level as a protective coating before FIB milling. The Ga signal is from the Ga ions used in FIB, and the C signal is from the C film, which supported the TEM sample and from carbon contamination on the sample. The only element that was likely to be from the wafer process is Ti. As a result, Ti spectrum imaging was performed. Elemental distribution information of Ti was subsequently acquired based on integrated intensities of the Ti Kα X-ray and the Ti $L_{2,3}$ edge [14]. The resulting elemental maps are presented in Fig. 12(b). The maps reveal that the faint layer contains Ti. The layer consists of Ti that remains from the Ti seed deposition used during fabrication of the tungsten plugs, and left behind after post-W CMP (chemical–mechanical planarization). Based on this analytical result, the pressure applied on the CMP polishing pads was increased, after which such a bridging problem was not observed again.

In general, a map of the integrated core-loss intensities alone is not sufficient to indicate the elemental distribution, since the intensity is not only proportional to the areal density of the

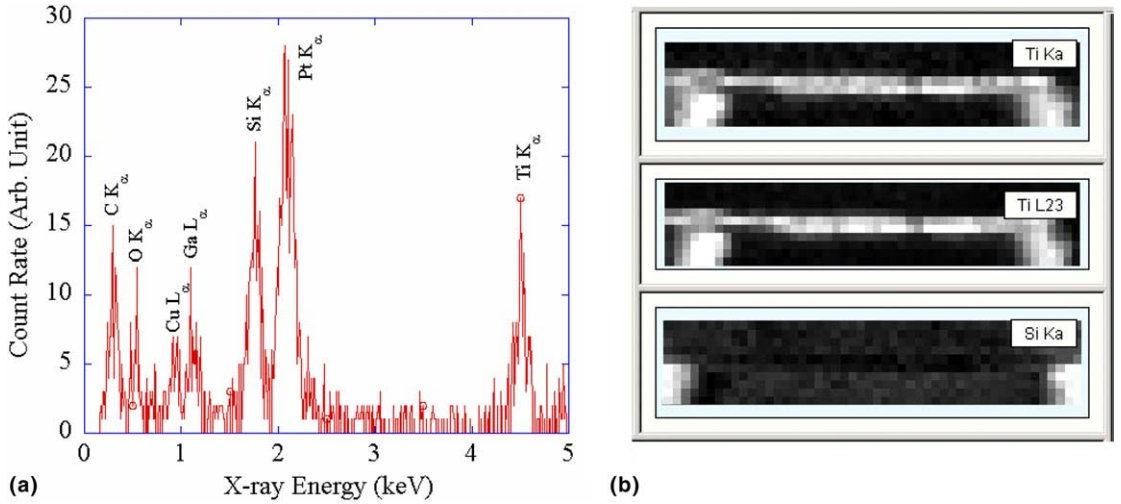


Fig. 12. (a) An EDS spectrum acquired from the faint layer between the two W-plugs. (b) Elemental maps of Ti based on integrated intensities of the Ti Kα X-ray and the Ti $L_{2,3}$ edge, and the Si Kα X-ray.

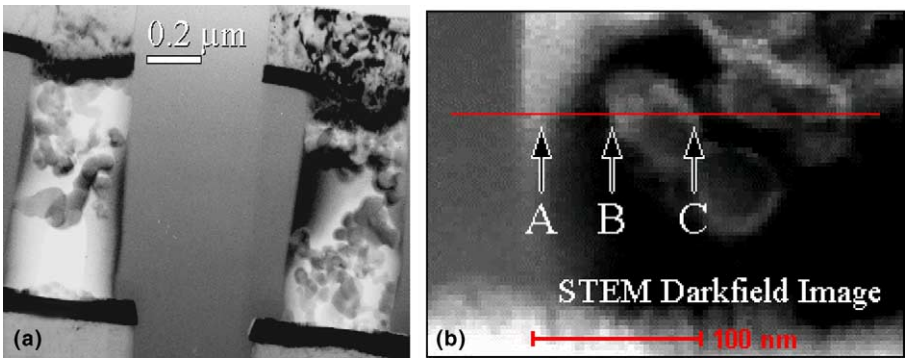


Fig. 13. (a) A TEM bright-field image of a pair of vias from a multiple bit failure site where the bits were electrically open. There is no metal via-fill, and clusters of particles are present in the vias. (b) STEM dark-field image of some particles in the bottom left corner of the right via, where EDS–PEELS spectrum profiling was performed. Three positions of the electron probe are labeled along the profile.

element projected along the electron transmission direction, but also the zero-loss intensity, which in turn decreases when the local mean free path of inelastic scattering, $\lambda$, becomes smaller. In our case, $\lambda$ for either Ti or Ti oxide is smaller than that of the surrounding $SiO_2$. Hence the indication of an increased areal density of Ti in the faint layer compared with the surrounding $SiO_2$ remains valid even when the $\lambda$ of Ti or Ti oxide and $SiO_2$ are taken into account.

The PEELS and EDS Ti maps are almost identical between the W-plugs. However, they become significantly different where the plugs are. The distribution of Ti in these two areas becomes broader in the EDS map. However, this is an artifact resulting from the increased background caused by the more intense Bremstrahlung radiation due to the presence of the heavy element tungsten. In contrast, the PEELS elemental map is not susceptible to this artifact. The EDS Si map consistently shows a deficiency of Si along the faint layer. However, the Si EDS map becomes brightest where the two W-plugs are. This artifact actually arises from W Mα X-rays, which are too close in energy value to Si Kα, to be resolved in EDS.

Fig. 13(a) is a TEM brightfield image of a pair of vias from a multiple-bit failure site where the bits were electrically open. The image reveals that there is no metal via-fill, and clusters of particles are present in the vias. Fig. 13(b) is an STEM darkfield image of some of the particles (located in the bottom left corner of the via on the right in Fig. 13(a)), across which EDS–PEELS spectrum profiling was performed. Three positions of the electron probe along the profile are labeled, and these correspond to positions labeled in Fig. 14(a).

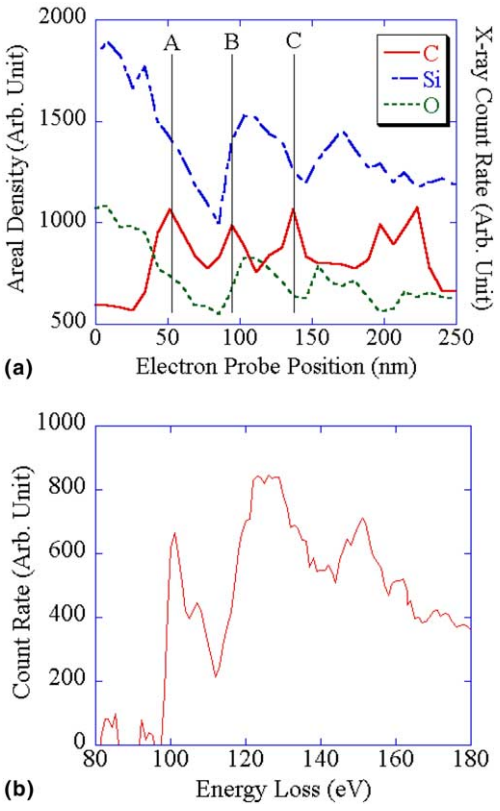


Fig. 14. (a) Profiles of the areal densities of C (acquired from PEELS), Si and O (obtained from integrated intensities of their Kα X-rays). (b) The $L_{2,3}$ edge of Si observed from the particle between positions B and C of the electron probe.

The areal density of C was calculated from the integrated C K edge [10], and in the profile is shown in Fig. 14(a) together with the integrated intensities of Si and O Kα X-rays. In Fig. 14(a), the variations of Si and O areal densities are almost entirely "conformal" in the particle between positions B and C, and in that to the right of position C. On the other hand, C areal density reaches local maxima at positions A, B and C, which are at the sidewall of the via, and the edges of the particle between B and C, respectively. The analysis showed Si and O are present in the particles, and C between the particles. This is consistent with an observation of the $L_{2,3}$ edge of Si in $SiO_2$ in the particle between positions B and C, which is shown in Fig. 14(b) [14].

The above observations suggest that after opening of the vias, there was remnant photoresist in the vias. The remnant photoresist prevented the filling of the vias by TiW. In addition, subsequent CMP introduced $SiO_2$ particles from the ILD (interlayer dielectric) into the via.

## 4. Conclusions

Focused Ion Beam in situ milling is a powerful technique used for failure analysis of memory-array bit failures. In standalone mode, and also combined with TEM/STEM, this technique allows identification of failure root causes, traceable to the fabrication process. Several failure mechanisms have been identified (killer particles, incomplete etching, pattern issues, incomplete CMP), and have led to appropriate process adjustments and yield enhancements.

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