Characterization Techniques for Evaluating Strained Si CMOS Materials

Qianghua Xie*, Ran Liu*, Xiang-Dong Wang*, Michael Canonico*, Erika Duda*, Shifeng Lu*, Candi Cook*, Alex A. Volinsky*, Stefan Zollner*, Shawn G. Thomas+, Ted White#, Alex Barr#, Mariam Sadaka#, and Bich-Yen Nguyen#

** Advanced Products Research and Development Laboratory, DigitalDNA Laboratories, Motorola, 2100 E Elliot Road, MD EL622, Tempe, Arizona, 85284*

+ Si RF/IF Technologies, DigitalDNA Laboratories, Motorola, 2100 E Elliot Road, MD EL741, Tempe, Arizona, 85284

 # Advanced Products Research and Development Laboratory, DigitalDNA Laboratories, Motorola, 3501 Ed Bluestein Boulevard, MD K10, Austin, Texas, 78721

Abstract. The electron and hole mobility of Si complementary metal on oxide field effect transistors (CMOS) can be enhanced by introducing a biaxial tensile stress in the Si channel. This paper outlines several key analytical techniques needed to investigate such layers. Raman scattering is used to measure the strain in the Si channel as well as to map the spatial distribution of strain in Si at a lateral resolution better than 0.5 µm. Atomic force microscopy (AFM) is used to measure the surface roughness. Transmission electron microscopy (TEM) is used to reveal dislocations in the structure, the nature of the dislocations and the propagation of the dislocations. Secondary ion mass spectrometry (SIMS) is used to monitor the Ge content profile in the structure and the thickness of each layer. In the long term, inline nondestructive techniques are desired for epi-monitoring in manufacturing. Two techniques, spectroscopic ellipsometry (SE) and x-ray reflectivity (XRR), have shown promise at this stage.

INTRODUCTION

The electron and hole mobility of Si complementary metal on oxide field effect transistors (CMOS) can be enhanced by introducing a bi-axial tensile stress along the wafer surface in the Si channel [1]. The physics for this improvement originates from reducing the effective masses, and the scattering of the holes and electrons by tailoring the band-structures [Figures 1(a) and (b)]. This provides an alternative route towards faster transistors, which are generally achieved by shrinking the gate lengths. While operational strained Si CMOS devices have been demonstrated on a R&D scale [2,3], the success of this technology in manufacturing relies on fabricating qualified strained Si on relaxed SiGe buffer layers. The strained Si wafer has a basic structure as follows: a few µm step or linear graded SiGe buffer layer was first grown on the Si substrate. Subsequently, a SiGe buffer layer having constant Ge content was grown followed by a strained Si channel of ~ 100-300 Å thickness [Fig.2 (a)]. Material requirements include, low defect density to constrain the leakage, low surface roughness to ensure that the strain-enhanced carrier mobility will not be compromised by interface

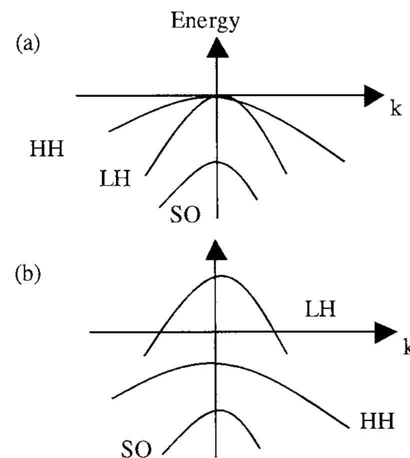

FIGURE 1. (a) is a schematic picture of the valence band structure of non-strained Si. (b) shows the band structure of Si under tensile stress. This stress causes splits in band sand thus reduces the band gaps and effective masses. In addition, the six-fold conduction band degeneracy is lifted which helps to reduce the inter-valley scattering.

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scattering, uniform spatial strain distribution and Si channel thickness to have devices with the same level of performance enhancement, and thermal stability [Figures 2(a) to (d)]. To address the challenges in characterizing the strained Si material, the International Technology Roadmap for Semiconductor (ITRS) is researching and defining appropriate metrology techniques.

Using a few strained Si wafers having a generic layer structure, this paper outlines several key analytical techniques. Raman scattering is used to measure the strain in the Si channel as well as to map the spatial distribution of strain in Si channel at a lateral resolution better than 0.5 μm. Atomic force microscopy (AFM) is used to measure the surface-roughness. Etch pit density (EPD) measurement was done to reveal the defects in the wafers. Transmission electron microscopy (TEM) is used to reveal dislocations in the structure, the nature of the dislocations and the propagation of the dislocation. The EPD/TEM data have been effectively used to optimize the strained Si material growth process to achieve low defect density. For the epi-growth monitor, we mainly employ secondary ion mass spectrometry (SIMS) to monitor the Ge content profile in the structure and the thickness of each layer. In the long term, inline nondestructive techniques are desired for epi-monitoring in manufacturing. Two techniques, spectroscopic ellipsometry (SE) and x-ray reflectivity (XRR), have shown promise at this stage.

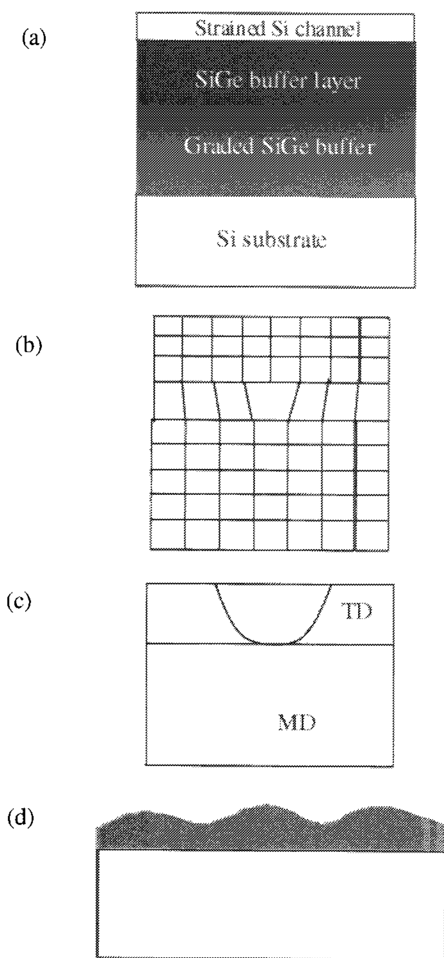

FIGURE 2. (a) shows a generic strained Si epi-stack having a graded SiGe and a constant SiGe buffer layer followed by a strained Si channel. (b) shows the creation of a misfit dislocation at a hetero-interface to accommodate the lattice mismatch. (c) shows a MD with a finite length turning into two threading segments. (d) shows the development of surface roughness.

EXPERIMENTAL

Raman scattering utilizes the phonon frequency shift in Si to detect the strain in the Si channel [4]. Raman measurements were performed on an UV-upgraded triple spectrometer in the subtractive configuration. Laser used for excitation is the 325 nm line from a He-Cd ion laser. The detector is a LN_2 cooled UV-enhanced (2048x512) CCD (spatial mapping of the strain is possible). The SIMS analyses were performed using a quadrupole-based low energy instrument with an attachment of a red laser diode (wavelength 670 nm and a spot size of ~ 2 mm) for charge neutralization, known as optical conductivity enhancement (OCE) [5]. This allows Ge composition quantification to a required precision of 0.5 at %. Atomic force microscopy (AFM) in conjunction with etch-pitch-density measurement can provide direct information on surface roughness as well as the TD density close to the active region. Atomic force microscopy (AFM) images were obtained on an atomic force microscope in the tapping mode. The tool has a sub-Å height resolution and better than 10 nm lateral resolution, which ensures reliable monitoring of surface quality and defect detection. TEM was carried out in an electron microscope equipped with a field-emitting electron gun (FEG) operating at 200 kV. Bright field images were taken with g=(004) to show the layer thickness and with g=(220) to best reveal the dislocations [6]. Plan view TEM was also performed to have a statistical measurement of the density of dislocations and defects close to the surface. For non-destructive monitoring of the wafer stacks (strained Si channel thickness), spectroscopic ellipsometry has great potential [7]. Variable angle spectroscopic ellipsometry (VASE) analysis was completed. Pseudo-dielectric functions ε_1 and ε_2 were measured from 0.74 to 6.6 eV with 0.02 eV steps at three incidence angles: 65°, 70°, 75°. The experimental data were modeled with a stack

consisting of: SiO_2 surface layer/Si (bulk Si optical constants)/ graded SiGe layer/Si substrate. The Si cap, oxide/surface roughness, and germanium concentration were determined from best fitting of the SE spectra. X-ray reflectivity (XRR) is a useful technique for measuring thin film thickness [8]. Strained Si wafers were measured using a diffractometer configured for X-ray reflectivity measurements. A 100 µm slit is placed at the X-ray source, and two 200 µm slits are placed in front of the detector. The incident beam is 100 microns wide and 10 millimeters long. The data is taken at angles, and at 40KV/40mA setting for the larger angles. The data were fit with a single Si layer on top of a SiGe bulk layer using commercial software to obtain film thickness, density and layer roughness.

RESULTS AND DISCUSSIONS

Figure 3 (a) shows typical UV-Raman spectra of the Si LO phonon in the strained Si cap and an unstrained Si reference. The vertical arrow marks the Si-Si LO frequency at ~ 513.7 cm^{-1} for a strained Si cap on a fully relaxed SiGe buffer layer with targeted 22% Ge composition derived from SIMS. From the data, it is estimated that 79.3% of the maximum possible strain has been achieved. Fig. 3 (b) shows a UV-Raman stress map for the sample. A clear stress pattern emerges along the <110> directions being coincident with the cross-hatch patterns observed by AFM. The lateral scale of stress variations is on the order of 5 µm in the Raman maps, also being close to the cross-hatch patterns in the AFM images. Based on binning the stress values from each pixel, the statistical mean stress is 1.14 ± 0.02 GPa with a range of 0.09 GPa for the sample. From Raman data, we have derived a tensile strain in Si channel (in-plane) in the range of 0.5% to 0.8% for most structures investigated.

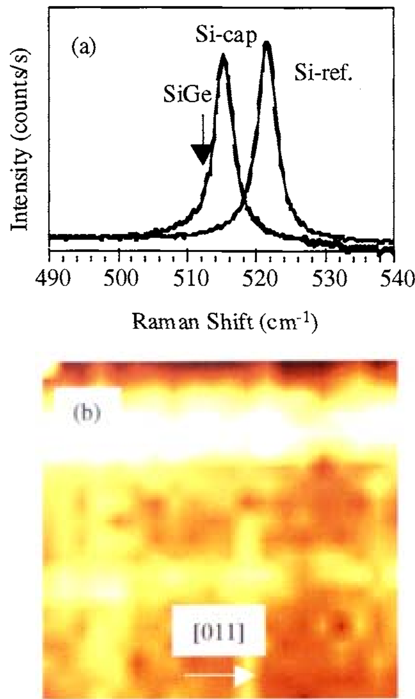

FIGURE 3. (a) shows the Raman spectra for a strained Si sample and an unstrained Si reference . The stress in the Si cap can be measured from the phonon peak shift. (b) shows spatially resolved UV-Raman stress mapping of the Si cap stress within an area of 10 µm ×10 µm. Features along the (011) direction are seen which could correspond to the cross hatch pattern seen by AFM. The range of stress is from 1.10 GPa to 1.18 GPa with a standard deviation of ~ 15%.

Fig. 4(a) is a XTEM picture taken under g=(022) reflection to reveal the distribution of the dislocations in the structure. It is seen that most of the dislocations are

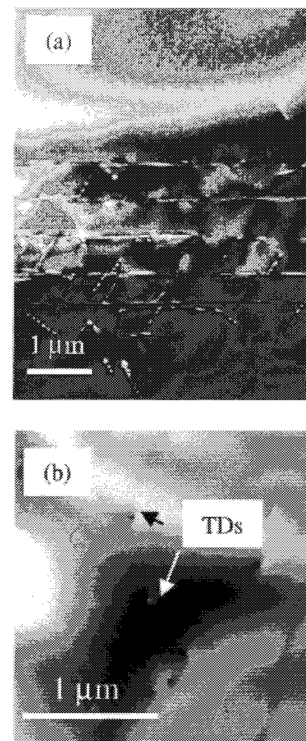

FIGURE 4. (a) is a XTEM of a strained Si sample. Most of the dislocations are confined in the graded buffer and step graded interfaces are revealed. The top SiGe constant buffer appears to be defect free (i.e. below the detection limit of TEM). (b) is a plan view TEM image, revealing the threading dislocations which are also seen in EPD measurements.

confined in the SiGe graded buffer layer and the MDs appear to coincide with the seven Ge grade steps in this structure. As discussed in Fig. 2(b), the misfit dislocations will turn into threading dislocations with vertical threading arms. The plan view TEM image shown in Fig. 4(b) reveals such threading dislocations close to the surface. This area has a particularly high TD density. In Fig. 5(b), a similar dot type of contrast is seen under an optical microscope for a sample etched for a few minutes for etch-pit measurement. It is suspected that the dot type optical image contrast and TD have the same structural origin. TEM is good for qualifying higher density of dislocation ($>10^6/cm^2$). For lower density, while TEM is good for studying the nature of the defects, it is not statistically reliable due to the limited sampling area of TEM images. EPD maybe a better technique for qualifying lower defect density.

Fig. 5(a) is an AFM image of an as-grown strained Si wafer. The surface roughness (RMS) is about 3.6 nm with clearly resolved cross hatch patterns along the (011) orientations. The stress variation and cross-hatch patterns are not desired since they may cause variation in the mobility enhancement for devices at different areas. Fig. 5(b) is an optical image showing the etch pits which are likely due to the threading dislocations close to the surface. With both the AFM and TEM analysis, the growth and process conditions of the strained Si wafers may be optimized.

Figs. 6(a) and (b) show the SIMS profiles of two wafers having step-graded and linear-graded SiGe buffer layers, respectively. Such SIMS data is important for process control of the SiGe growth. As an example of the deviation from the desired growth, super- or sub-linear Ge profiles have been observed in SiGe buffer layer by SIMS for ill-tuned epitaxial growth processes.

Fig. 7(a) displays the dielectric functions (ε_1 and ε_2) over the photon energy range 1.0 eV to 6.0 eV derived from SE. By fitting the SE data using optical constants of non-strained Si and relaxed SiGe, we obtain best agreement with 13% Ge and 20 nm Si channel. The Ge content measured by SIMS for this sample is about 20% and a Si channel thickness of 15 nm was measured by TEM. The discrepancy between the actual Ge percentage and Si cap thickness and those fit with SE, is likely due to the optical constants used here where the influence of stress on the Si optical constants was neglected.

Fig. 7(b) displays the experimental and simulated XRR data for a strained Si wafer. The two spectra have been vertically displaced for better presentation. It is seen that the simulation and experiment match well with each other with Si cap thickness of 172 Å as

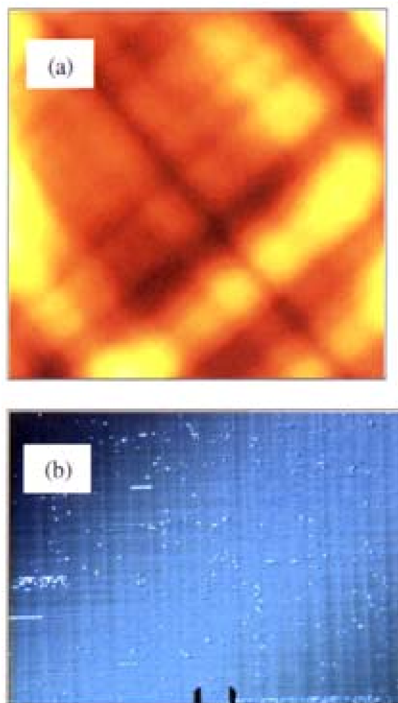

FIGURE 5. (a) is a top view AFM image of an as-grown strained Si sample, having RMS of 3.6 nm. (b) is an optical image of a sample etched by about 2000 Å revealing TD close to the surface. The mark represents 10 μm.

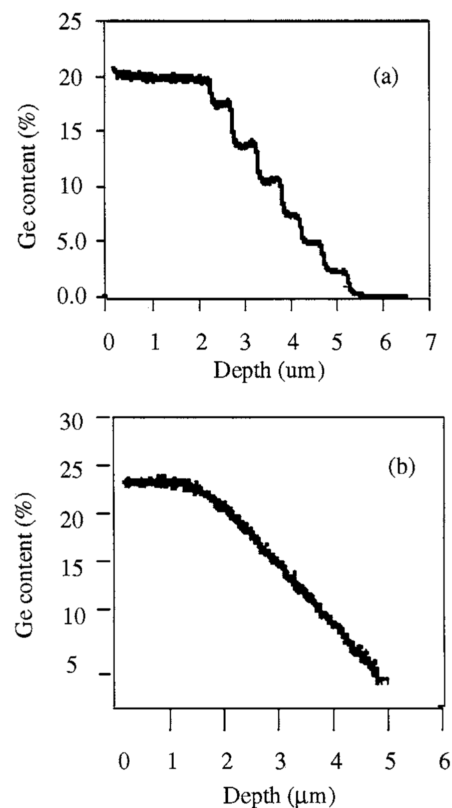

FIGURE 6. (a) and (b) are the SIMS profiles showing two strained Si wafers having step-graded and linear-graded SiGe buffer layer, respectively.

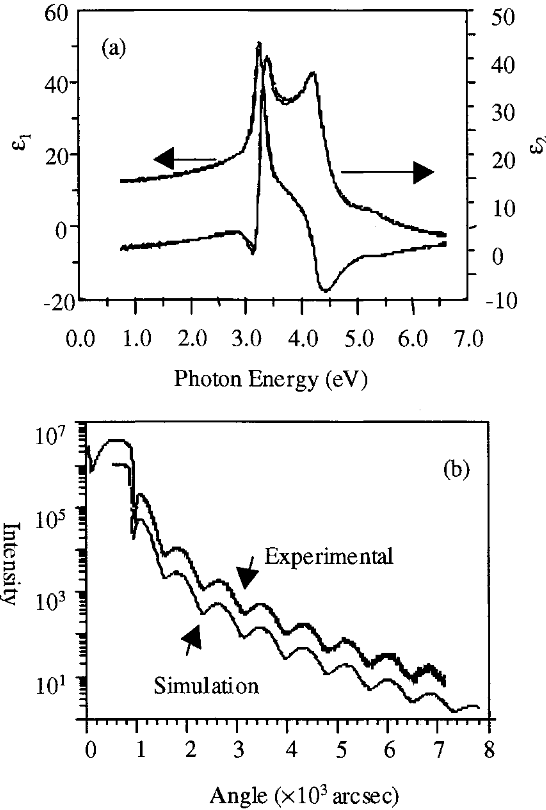

FIGURE 7. (a) shows the pseudo-dielectric function for a strained Si wafer. To fit the data using bulk Si and bulk SiGe, the following set of data yields good results, 20 nm Si channel, 13% Ge, 2 nm surface overlayer (oxide/roughness). (b) includes XRR data (experimental and simulation) for a strained Si wafer, which match well with each other.

compared to 165 Å measured by TEM. In the fitting, a surface oxide layer of 14 Å has also been included, consistent with the surface oxide on a scale of 20 Å revealed by TEM.

SUMMARY

With the understanding of the material requirements of the strained Si channel CMOS, a comprehensive set of analytical techniques are outlined to address these material issues. Raman scattering measures the strain in Si cap and the stress distribution. AFM/TEM/EPD help to define the strategy for defect reduction. SIMS, SE and XRR have shown promise to serve as critical epi-monitoring tools.

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