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Gate oxide metrology and silicon piezooptics☆

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Abstract

We describe the use of spectroscopic ellipsometry and other characterization techniques for gate oxide process metrology in manufacturing of CMOS transistors for the 130 nm node and beyond. Specifically, we describe the difficulties associated with the introduction of silicon-on-insulator (SOI) substrates, alternative gate dielectrics (silicon oxynitride or metal oxides), and strained Si channels. We predict that spectroscopic ellipsometry by itself will no longer be sufficient for gate oxide metrology, which will make the CMOS gate stack process much more difficult to control.

Keywords: Gate oxide metrology; Spectroscopic ellipsometry; Strained Si; Piezo-optic tensor

1. Introduction to ULSI gate oxide metrology (thermal SiO_2)

The fabrication of complementary metal-oxide-semiconductor (CMOS) field effect transistors (FETs) for ULSI technology starts with the oxidation of the bare Si substrate, conventionally through thermal oxidation [1]. Accurately measuring the thickness of this gate oxide is crucial, since it determines the electrical properties of the transistor [2]. For older CMOS generations, the SiO_2 thickness on Si was quite large, which made the thickness measurement very simple, even based on the ellipsometric angles only at a single or a few wavelengths (sometimes taken at multiple angles of incidence by focusing the beam and using photodiode array detection). The optical constants of Si and SiO_2 are well established over a broad range of wavelengths, therefore the oxide thickness is the only adjustable parameter when fitting the ellipsometric angles (since the interfaces are smooth). For thinner layers, spectroscopic ellipsometry in the UV is more accurate than in the visible due to the enhanced surface sensitivity of the imaginary part of the pseudodielectric function in the vicinity of the E_2 critical point near 4.2 eV. At least theoretically, sub-Å precision is possible. In practice, there are two problems for very thin oxides with thicknesses below 30 Å: First, the oxide is usually covered with adsorbed water vapor or thin organic films (atmospheric molecular contamination from the factory environment), which add to the measured total thickness [2]. This can be overcome by heating the wafer to a sufficiently high temperature to desorb the overlayer, which is still low enough to avoid additional oxide growth. This heating step can be performed outside the ellipsometer (just before measurement) or inside a nitrogen-purged enclosed ellipsometer with a heatable wafer chuck. Measurements of the heated substrate are also possible, if the temperature dependence of the optical constants for Si and SiO_2 is taken into account. The second problem is that the refractive index of SiO_2 may increase for small thicknesses due to quantum confinement effects. Therefore, the gate oxide thickness is often quoted as an 'optical thickness', i.e. the thickness determined from the ellipsometric angles when neglecting the dependence of the refractive index on thickness, in contrast to the 'electrical thickness', i.e. the thickness determined from capacitance–voltage measurements (where the oxide is sandwiched between the Si substrate and a doped poly-crystalline Si layer to form a capacitor or MOSCAP) or the 'physical thickness' that one would obtain from transmission electron microscopy (TEM). Except for the thickness dependence of the refractive index of SiO_2, the optical and physical thickness should agree. The capacitor electrical thickness (CET) is slightly larger, since the depletion widths in the substrate and the gate need to be added.

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The success of spectroscopic ellipsometry in the semiconductor industry for gate oxide metrology explains the large number of instruments sold.

2. Difficulties associated with silicon-on-insulator substrates

To improve performance, modern devices are often built on silicon-on-insulator (SOI) wafers consisting of the Si substrate, a buried oxide (BOX, 100–200-nm thick), and a crystalline top Si layer (or body), also 100–200-nm thick. Such materials can be produced by ion implantation followed by annealing (silicon implanted with oxygen, SIMOX) or wafer bonding followed by processing to thin the sacrificial wafer. Measuring the gate oxide thickness on SOI is still simple [3]. The Si body is much thicker than the penetration depth of the light at the E_2 critical point, therefore the presence of the BOX can usually be neglected when analyzing the UV portion of the spectrum. For Si thicknesses greater than 5–10 nm, the influence of confinement on the UV portion of the spectrum can be neglected, but some broadening of the E_1 critical point is possible. The infrared and visible portions of the spectrum (below and near the E_1 edge) carry information about the thicknesses of the BOX and body. Optical metrology for the SOI starting material is similar. In the data analysis, one simply considers the native oxide instead of the gate oxide. For the analysis of oxides over SOI, it is important to consider the depolarization of light in the ellipsometry measurements. In most cases, the depolarization spectrum is dominated by the finite resolution of the monochromator. Thickness non-uniformity of the BOX or the Si body can also contribute, if these parameters are not well controlled. The refractive index of the BOX should be the same as that of SiO_2. A slightly higher refractive index can be explained by the presence of Si precipitates in the BOX.

3. Difficulties introduced by alternative gate oxides

Scaling CMOS devices to follow Moore's law requires thinning the gate oxide layer. For modern devices, this leads to problems, as the gate-channel leakage currents (tunneling through the oxide) become significant. Instead of thinning the oxide, one increases the dielectric constant of the oxide, which also increases the areal capacitance. At present, this is achieved by adding nitrogen to the oxide, forming a silicon-oxynitride (SiON) gate oxide [1,2]. (This also helps to reduce diffusion of dopants through the thin oxide.) Since the refractive index of SiON depends on the N content, we notice immediately that ellipsometry alone can no longer determine the properties of the oxide (thickness and composition) for very thin films, since it only measures the product of thickness and refractive index for very thin films. For additional information, other techniques providing elemental information are needed, such as X-ray photoelectron spectrometry, secondary ion mass spectrometry or other surface science techniques. FTIR ellipsometry and attenuated total reflectance (ATR) FTIR spectroscopy are also promising, since the Si–O and Si–N vibrations lead to absorption in distinctly different wavelength regions. An additional complication is the non-uniform N distribution throughout the film, depending on preparation methods. For example, when depositing SiON on a Si wafer covered with native oxide, there may not be any N near the substrate. Annealing SiO_2 in nitrogen may lead to different properties than growing the thermal oxide in a nitrogen-containing ambient. At present, gate oxide metrology of SiON gate dielectrics is an unsolved problem.

To increase the dielectric constant of the gate oxide even further, allowing an electrical thickness of 1–2 nm with a physical thickness of 5–10 nm, SiO_2 is replaced by metal oxides, such as HfO_2, $HfSiO_4$ or $LaAlO_3$. Deposition of such metal oxides by chemical vapor deposition (CVD), atomic layer deposition (ALD) or physical sputtering usually produces (or leaves behind) an SiO_2 interfacial layer between the Si substrate and the metal oxide. In this case, gate oxide metrology consists of determining the thickness of the interfacial layer and the metal oxide [2,4]. It is desirable to also determine some properties of the interfacial layer (which could be an intermediate oxide or silicate). This is a very difficult problem with ellipsometry alone (without other analytical techniques providing additional information). One cannot assume that the optical constants of the interfacial layer or the metal oxide are well known. For example, annealing of the metal oxide in an oxidating or reducing environment may change the density of oxygen vacancies. Annealing and growth conditions also change the crystal structure. HfO_2, for example, can be amorphous, tetragonal or monoclinic. The crystal structure influences the dielectric function of the metal oxide, particularly near the band gap (typically in the range of 3–7 eV). Because of the high band gap of many metal oxides, VUV ellipsometry (up to 9.5 eV with a deuterium lamp) is very useful.

For a metal oxide of thickness 5–10 nm with a 1 nm thick interfacial layer, it is usually [4] possible to fit the ellipsometric angles from 0.7 to 6.6 eV at the three angles of incidence (60–75°) with a single layer. The output of the fit is thus the 'optical' thickness of the gate oxide and the dispersion. For crystalline materials such as monoclinic hafnia, a parametric oscillator model gives a good description of the dispersion. A Lorentz or Tauc-Lorentz model usually fails near the band gap for crystalline materials, but fits well for amorphous gate oxides. For layers with 5-nm thickness or below, the dispersion has a large uncertainty and is correlated with the thickness. The dispersion obtained from the fit needs

to be interpreted as an 'optical average' of the interfacial layer and the metal oxide. It will depend on the thicknesses of both layers and the experimental conditions (such as wavelength range). Since the refractive index of the interfacial layer (SiO_2) at 2 eV is usually lower than that of the metal oxide, the effective refractive index increases with increasing metal oxide thickness. We stress that ellipsometry alone cannot determine both thicknesses and that we cannot assume that the dispersion of the metal oxide is well known or even constant.

Since ellipsometry by itself has very limited capabilities for gate oxide metrology, other techniques have been explored as well. Since the wavelength of X-rays is much smaller than that of light in ellipsometry, X-ray reflectivity [2] has been explored for gate oxide metrology. For such measurements, it is crucial that the wafer is aligned very well and that the X-ray reflectometer has a high dynamic range. Both scanning and multiple-angle (with two-dimensional detector) X-ray reflectometers have been developed. However, it turns out that a reasonably good fit can often be obtained even with a single layer, just like in ellipsometry. Therefore, even X-ray reflectivity is not too sensitive to obtain both layer thicknesses, particularly if surface and interface roughness parameters are allowed when fitting the data. Just like in the case of oxynitride gate dielectrics, other techniques are needed for characterization, such as FTIR ellipsometry or ATR-FTIR spectroscopy, X-ray photoelectron spectrometry, secondary ion mass spectrometry or other surface science techniques. The suitability of each technique (validity of thicknesses determined) is compared with transmission electron microscopy, which has its own constraints.

4. Piezooptical effects in strained Si channels

Gate oxide metrology becomes even more complex, when high-mobility strained Si channel structures are used as the starting material instead of bulk Si or SOI wafers. Strained Si can be grown on thick relaxed SiGe buffer layers on bulk Si or on compliant substrates consisting of thin SiGe layers on SOI. In both cases, the metrology of the starting material is crucial with a large number of parameters to be controlled: (1) thickness and Ge profile of the SiGe buffer; (2) thickness of the strained Si channel; (3) roughness of the Si/SiGe interface and the Si surface; (4) magnitude and local variation of stress in the Si channel; (5) threading dislocation density in the Si channel (high sensitivity of the measurement is needed, since the desirable dislocation density is very low, $<10^3$–10^4 cm^{-2}); (6) density of other defects, such as twins, dislocation pile-ups or misfit dislocations, particularly at the SiGe/Si channel interface; and (7) distribution of dopants in channel and buffer (particularly after thermal annealing).

Transmission electron microscopy is readily available to determine thicknesses and interface/surface roughness on a microscopic scale. Both threading and misfit dislocations can be seen in TEM images, but TEM sensitivity to dislocations is poor because of the limited field of view. Atomic force microscopy determines the surface roughness of the Si channel. Etch pit density (EPD) measurements determine the density of threading dislocations near the surface. Clear prescriptions for EPD are needed to select the etch depth. The meaning of lines and points in the EPD optical images need to be explained. Computer-controlled data analysis of EPD images is desirable and under investigation. X-Ray topography is another technique offering promise for defect detection. The Ge and dopant profiles can easily be measured with SIMS. A high sputtering rate is needed for thick SiGe buffers, while high depth resolution (possibly with a low-energy floating ion gun) enables the analysis of the thin Si channel and of the channel/buffer interface. Optical carrier excitation using a laser

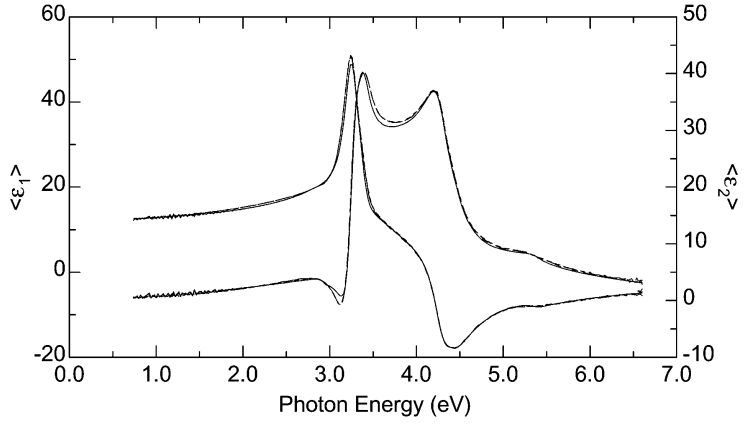

Fig. 1. Pseudodielectric function (dashed lines) of strained Si (15 nm, 1.3 GPa tensile stress) on a thick relaxed SiGe alloy buffer (20% Ge). Using optical constants for bulk Si and SiGe alloys, it is possible to achieve a reasonable fit to the data (solid lines), but the results (20-nm Si thickness, 13% Ge) are incorrect, since the influence of the stress on the optical properties has been neglected.

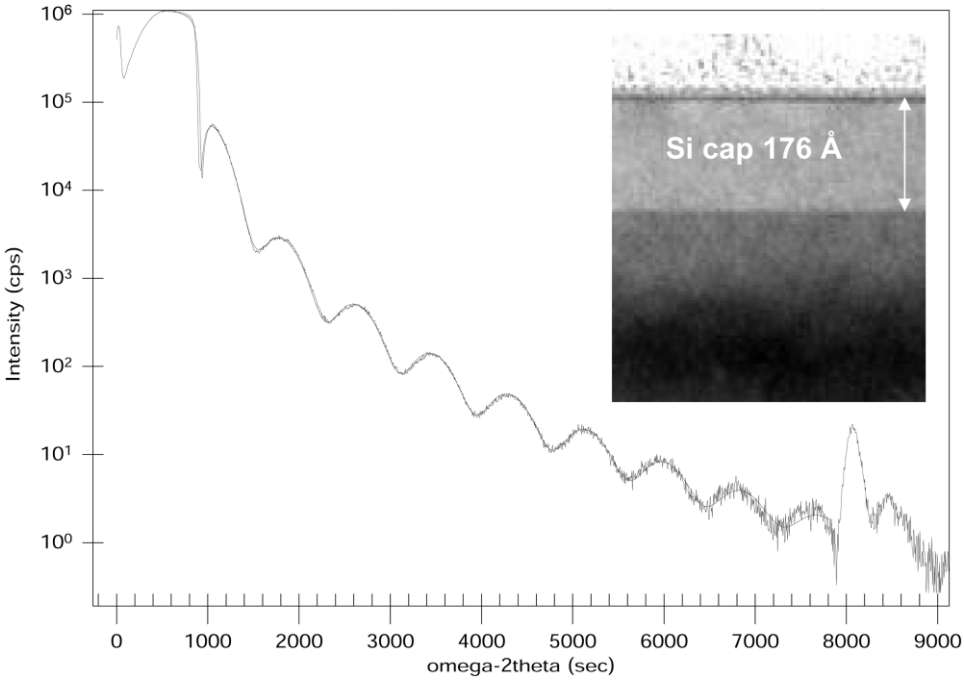

Fig. 2. X-Ray reflectivity scan for a strained Si layer on a thick SiGe alloy buffer. From the periodicity of the interference fringes, the thickness of the Si layer can easily be determined (172 Å), since the refractive index of Si for X-rays does not depend on stress. The inset shows a transmission electron micrograph, yielding a Si layer thickness of 176 Å. The peak at 8000 s is of unknown origin, presumably a small-angle diffraction peak.

diode directed at the sputtering crater avoids SIMS charging artifacts. This is particularly important for strained Si over SOI and for undoped layers.

Stress of the Si channel is the crucial parameter that determines the mobility enhancement of electrons and holes. Measuring this biaxial stress is possible using Raman spectrometry, since the energy of the Si–Si vibration in the Si channel depends on stress [5]. However, the phonon deformation potential (describing the variation of the Si–Si phonon energy with stress) is not firmly established for thin Si channels. Such Raman measurements need to be performed using a UV laser to avoid penetration of the laser into the Si substrate. At 325 nm wavelength, the entire Raman signal stems from the thin Si channel, which makes data analysis simple. For longer wavelengths, the Si–Si vibration in the SiGe buffer appears also. The energy of this vibration depends on alloy composition and stress, which provides additional information. Raman mapping yields the stress distribution across the wafer with a maximum resolution of approximately 0.5 μm, thus predicting transistor-to-transistor variations in mobility enhancements. It would be desirable to improve this resolution, possibly using solid or liquid immersion techniques.

Analysis of ellipsometry data for such strained Si channels is complicated, since the dielectric function of Si depends on the stress [6,7]. This relationship (described by the piezo-optical or elasto-optical tensors) is qualitatively understood, but we lack sufficiently accurate quantitative data for fitting ellipsometry data of strained Si channels to extract the Si channel thickness. The Si thickness is generally overestimated by approximately 35%. When fitting the ellipsometric angles of strained Si channel structures, poor agreement is usually found near the E_1 critical point, where the exact lineshape depends on stress, Si thickness and Ge content in the buffer [5–9], see Fig. 1. When only considering the UV portion of the ellipsometry spectra, there is some hope that we may be able to determine the gate oxide thickness, at least for sufficiently smooth surfaces. For rougher surfaces, there is an additional source of error, since the surface roughness enters the ellipsometry data analysis in a similar fashion as the native or gate oxide. For accurate gate oxide metrology, the Si surface roughness should be an order of magnitude less than the gate oxide thickness. This is satisfied for bulk Si starting materials, but may cause concerns for measurements on strained Si channels. Confinement effects in the thin Si channel are not yet an issue in the visible and UV portions of the ellipsometry spectra. In principle, ellipsometry should not only be able to determine the Si channel thickness, but also the Ge content of the SiGe buffer underneath. In practice, however, the Ge content determined from the data is much too low, possibly due to ignoring the strain effects on the Si

dielectric function. (On pseudomorphic Si/SiGe heterostructures, ellipsometry is much more successful.)

X-Ray reflectivity [2] is an attractive alternative to spectroscopic ellipsometry to determine the strained Si channel thickness, since the refractive index for X-rays is very close to 1 and does not depend on the stress. Indeed, see Fig. 2, for Si channel thicknesses of the order of 10–20 nm, a clear series of interference fringes (sometimes accompanied by an additional small-angle diffraction peak of unknown origin) is obtained. However, determining the Si channel thickness using commercial software fitting packages does not always yield the correct value (in comparison to TEM). Possibly, this is related to the surface roughness, which is more difficult to handle for X-ray reflectivity experiments than for spectroscopic ellipsometry because of the smaller wavelength. Experimental concerns about X-ray instrument reliability and alignment are similar to described above for measurements on high-*k* gate dielectrics. High-resolution triple-axis X-ray diffraction has been used successfully (using lab and synchrotron X-ray sources) to determine the vertical Si lattice constant in the channel, another measure for the stress in the structures.

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